Neverlast and Beyond

Handling Volatility in NVRAM-centric Operating Systems

GI Fachgruppe Betriebssysteme - Herbsttreffen
September 21, 2021

Christian Eichler[1], Henriette Hofmeier[1], Wolfgang Schröder-Preikschat[2], and Timo Hönig[1]

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RUHR UNIVERSITÄT BOCHUM

RUB

FRIEDRICH-ALEXANDER UNIVERSITÄT ERLANGEN-NÜRNBERG

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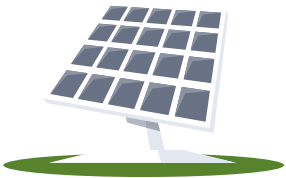

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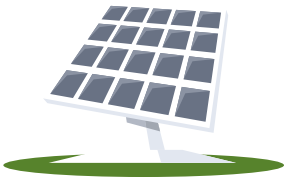

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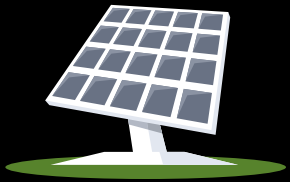

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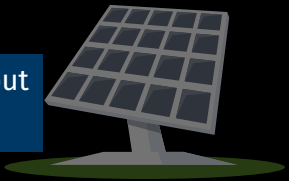
$\rightarrow$ Intermittently-powered systems may run out of power, but **must not lose system state**



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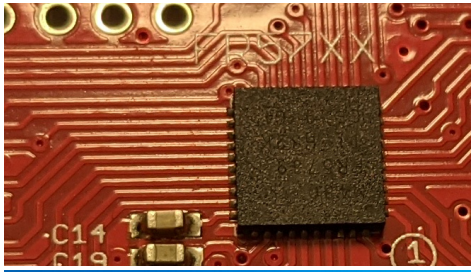

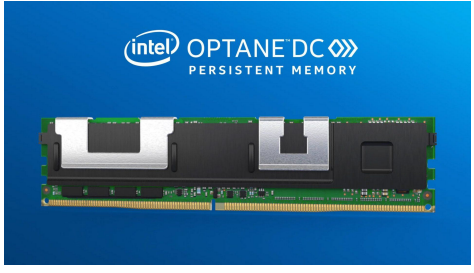

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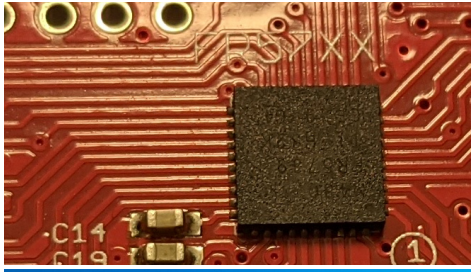
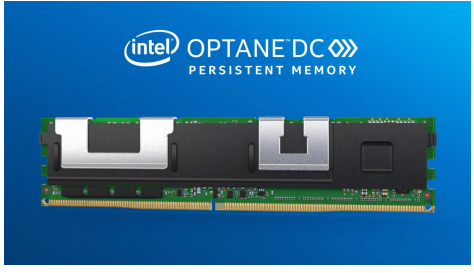
- – Hardware configuration





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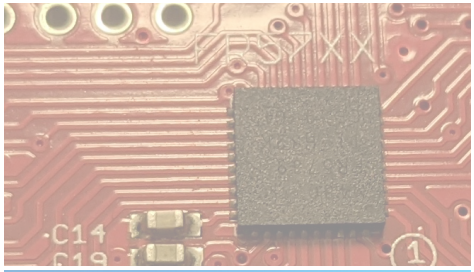

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→ **Data in volatile components** must be taken into account when persisting the system state

Motivation: Consistency is Key

Losing not-yet persisted volatile state leads to **inconsistent** system states [o].

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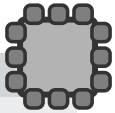

Sensor Configuration

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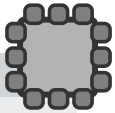

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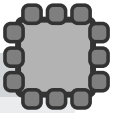

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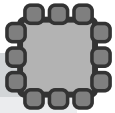

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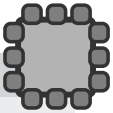

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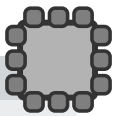

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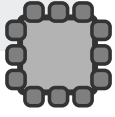

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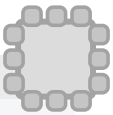

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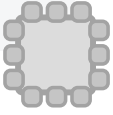

→ Losing **volatile state** eventually leads to **inconsistencies**

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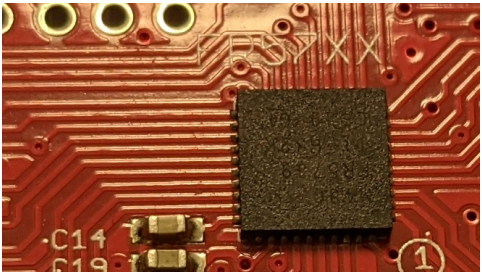
Design & Implementation of Neverlast

Neverlast: Handling Device and System Consistency

Consistency comprises...

- Application and OS data
- Volatile cache and register contents
- But also **volatile hardware configuration**



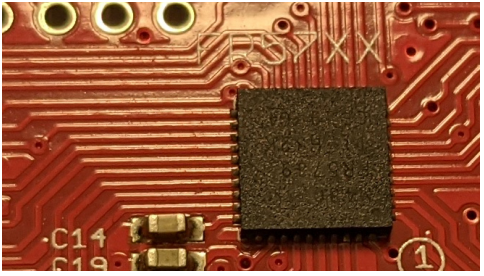
Therefore, Neverlast...

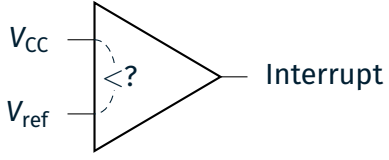
1. Minimizes the volatile state by running in NVRAM
2. Saves registers & caches on power outage
3. Traces device-configuration syscalls

Neverlast: Detecting & Handling Power Outages[1]

Detecting Power Outages

1. Voltage comparator monitors V_{CC} and interrupts the CPU when V_{CC} falls below threshold





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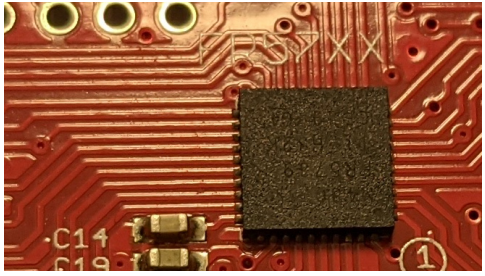

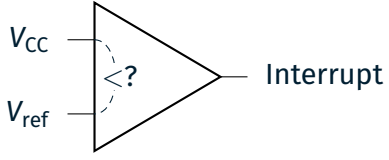

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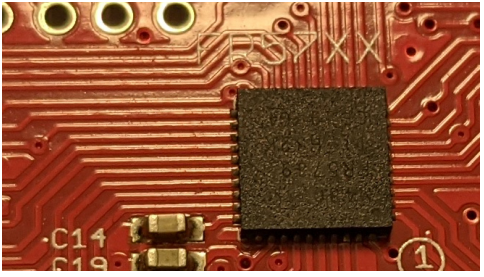
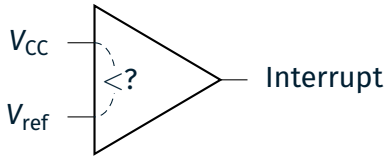


Recovering from Power Outages

1. Check stored system state for validity
2. Restore volatile state
3. Continue execution



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Neverlast's Approach: Trace System Calls

- Transaction-like behavior (via `replay_start` and `replay_stop`)
- Log system calls (including parameters) to persistent log
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→ Use **syscall-based transaction mechanism** for peripheral devices

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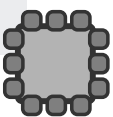

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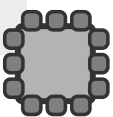

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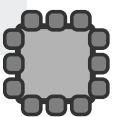

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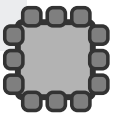
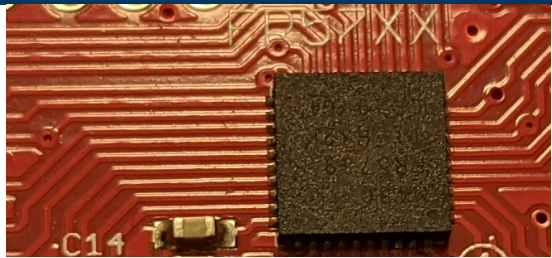
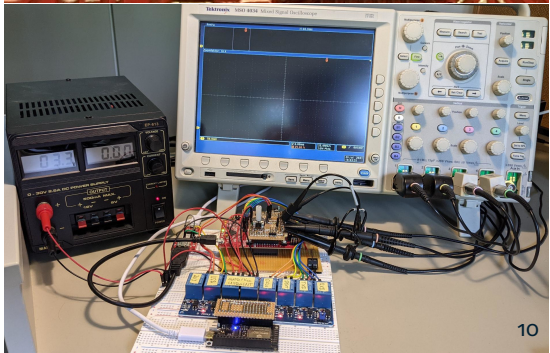


Evaluation

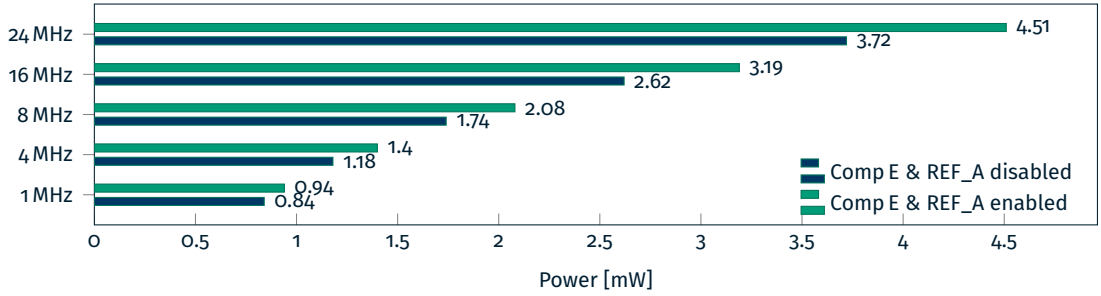
Evaluation - Setup

- MSP-EXP430FR5994 LaunchPad Development Kit
  - 16 bit RISC processor, up to 24 MHz
  - 8 KB of SRAM
  - 256 KB of FRAM with 2-way-2-line read cache (2x 8 Byte)
- Remote-controlled via relais card
- Shunt-based energy measurement Tektronix MSO 4034





Evaluation - Power Consumption by Supply Monitoring



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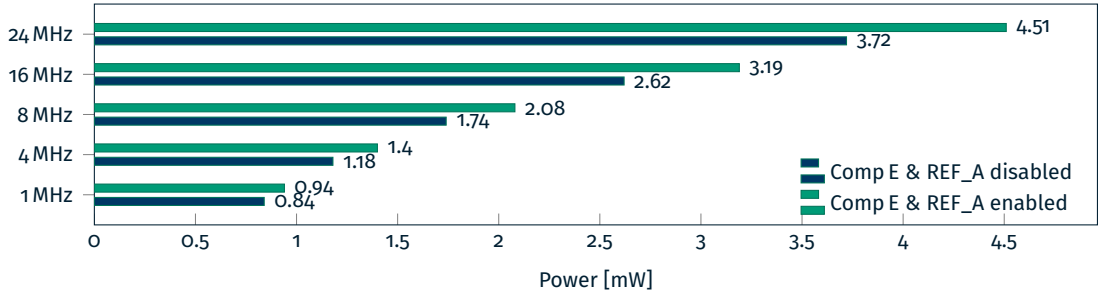

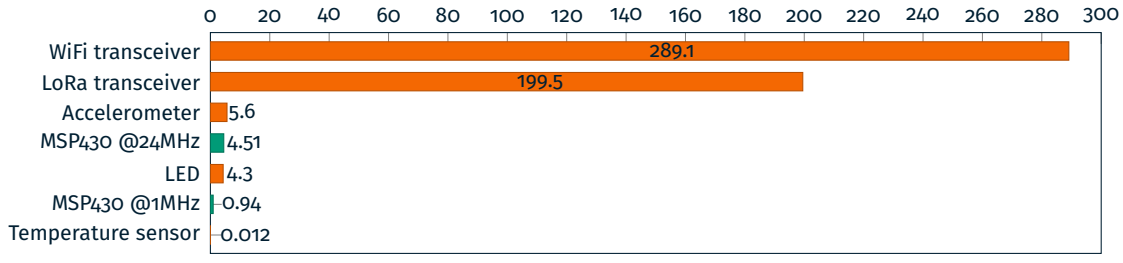

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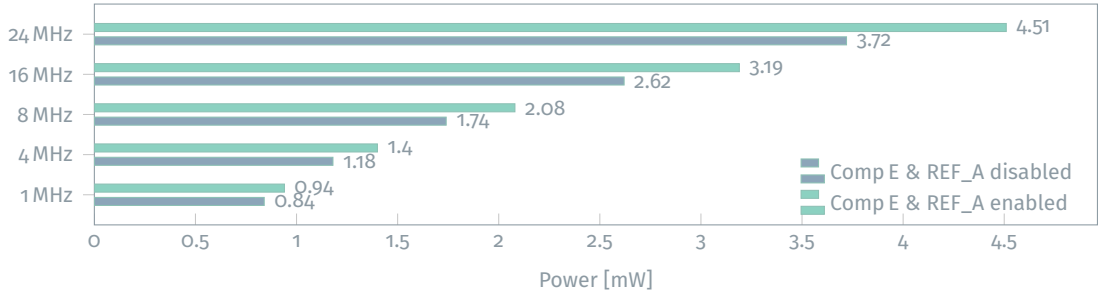
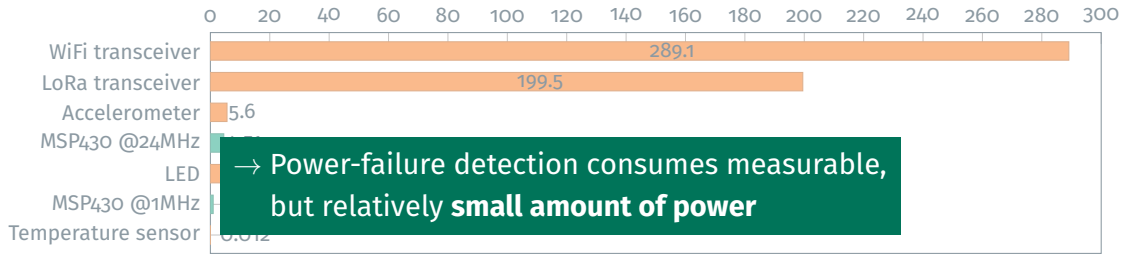
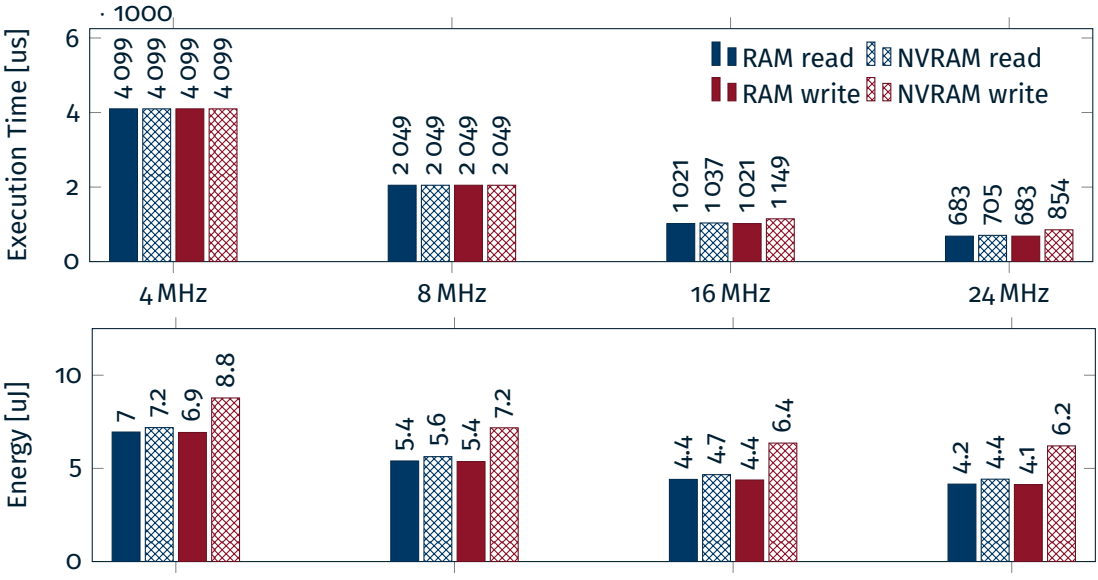




→ Power-failure detection consumes measurable, but relatively **small amount of power**

Evaluation - Performance of NVRAM vs. RAM (sequential read/write)



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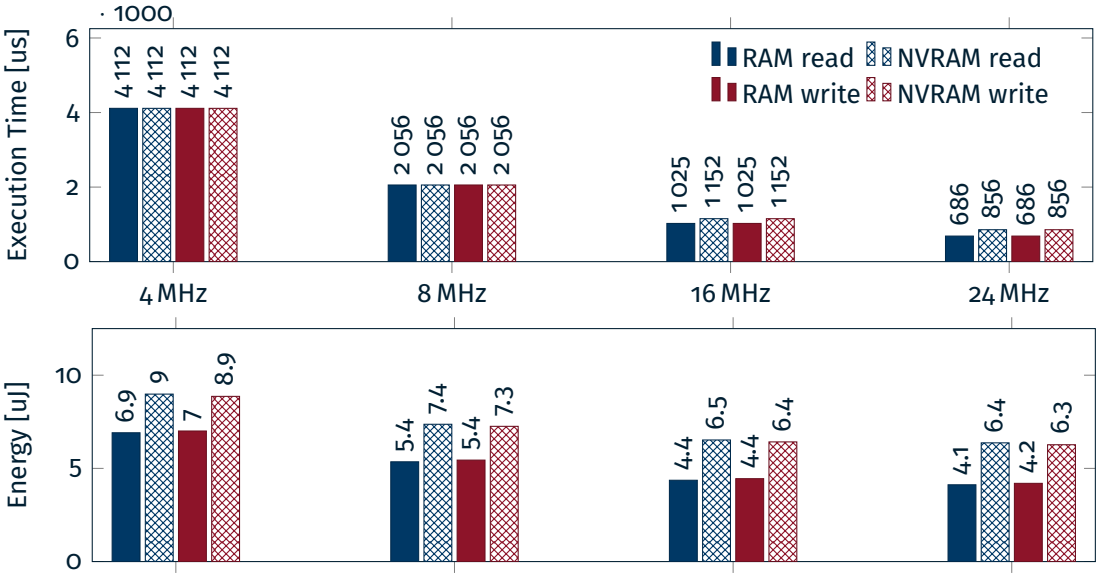

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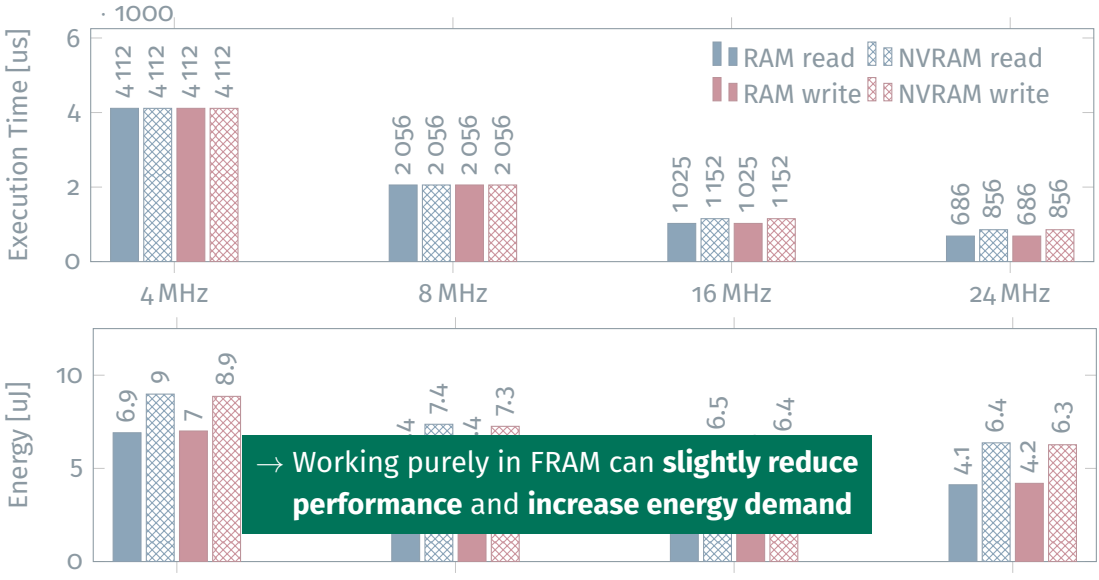

Neverlast – Conclusion

Systems with non-volatile memory (will) become more and more widespread, but come with **challenges**:

- ? Energy-harvesting systems may lose power anytime
- ? Consistency in systems with mixed volatility...
- ? and peripheral devices

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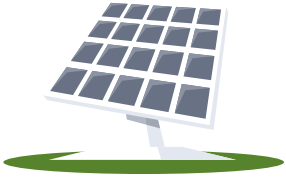

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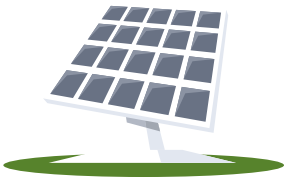

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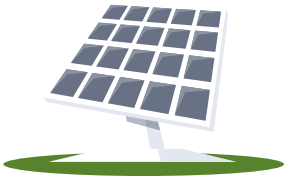
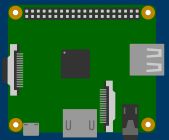
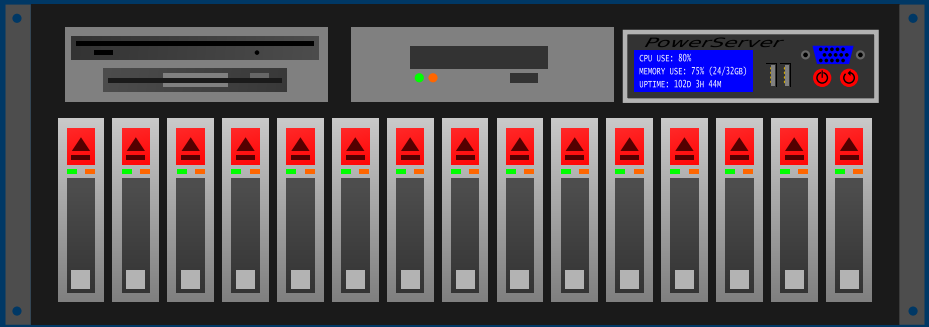
  → **Trace & replay** device-configuration syscalls



A Peak into the Future...



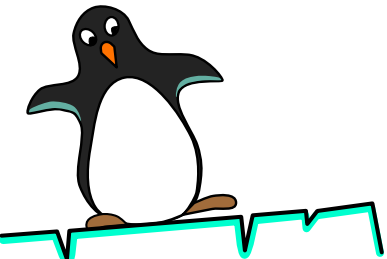


Operating Systems and their Memories

Persistent memory used to be (really) slow and high latency

- Think of: Mechanical hard drives
- OSes avoid persistent memory when possible

→ Use of volatile caches



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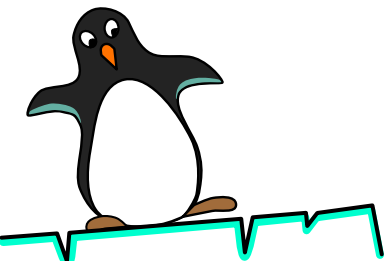
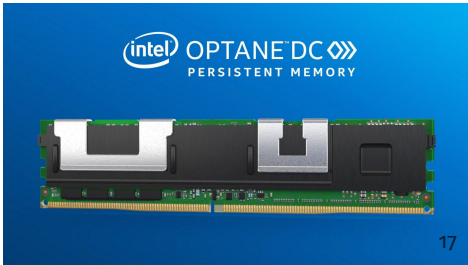


The OS handles RAM volatility in software:

- Periodic flush of write-back file caches
- Periodic flush of the superblock & inode cache
- „Hibernate to disk“

Running Linux in NVRAM – without Volatile RAM

Imagine using (only) non-volatile main memory:



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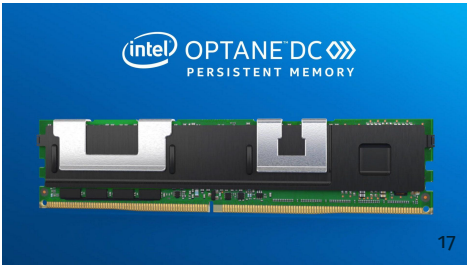

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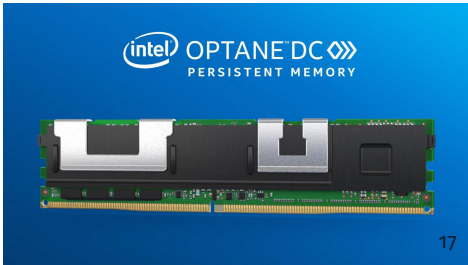

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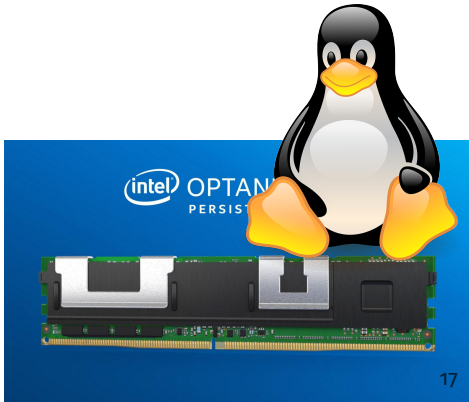
- DFG NEON / Linux on Intel Optane:
  - Port Neverlast's ideas to Linux
  - Identify & remove obsolete persistency measures



Conclusion

NVRAM-centric operating systems come with **challenges and opportunities**:

- ? Persistency & consistency in presence of volatile components
- \+ Optimization of the OS:
  - \+ Simplifications
  - \+ Reduced TCB
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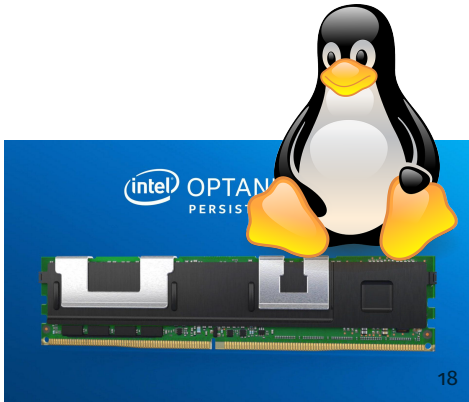

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