CLoF: A Compositional Lock Framework for Multi-level NUMA Systems



March 18th, 2022

Concurrency is Everywhere

Modern operating systems, databases & applications resort to **multi-core concurrency** to achieve high performance.



Concurrency is Everywhere

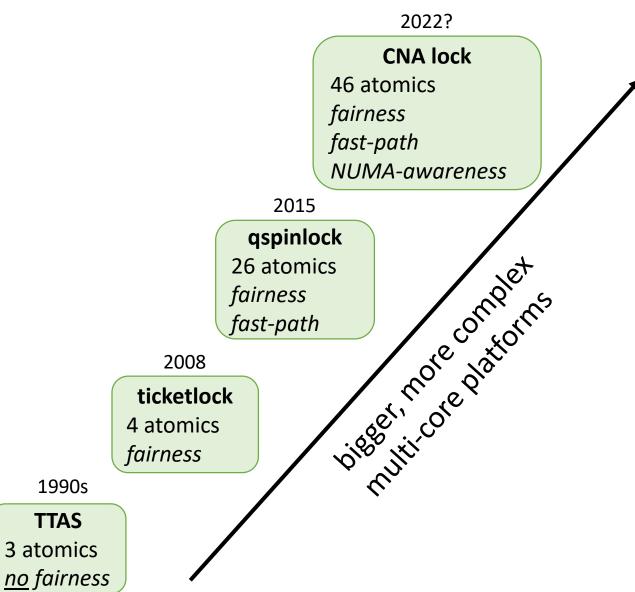
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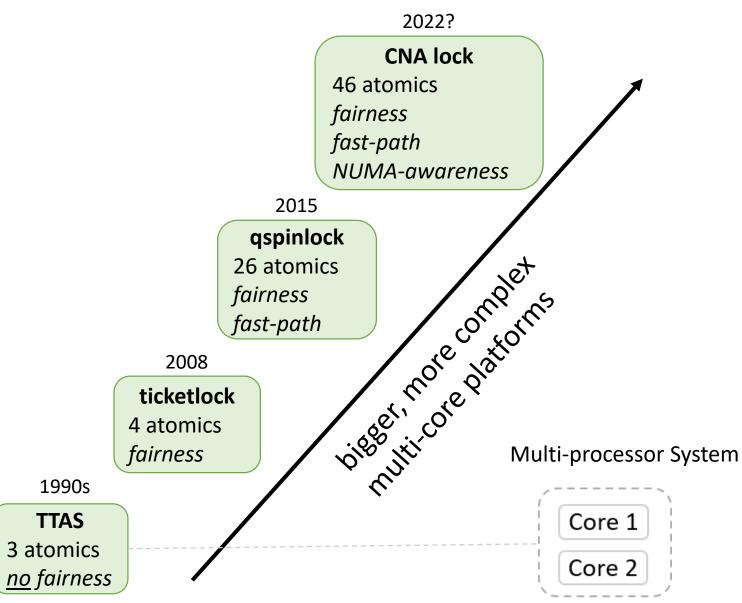
Multi-core concurrency:

One of its most important tasks is to *synchronize* access to shared variables

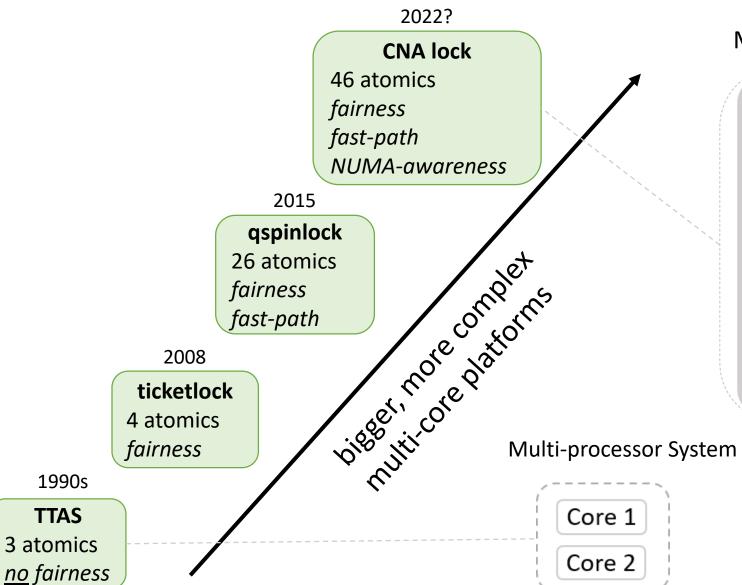
Linux spinlock evolution



Linux spinlock evolution



Linux spinlock evolution



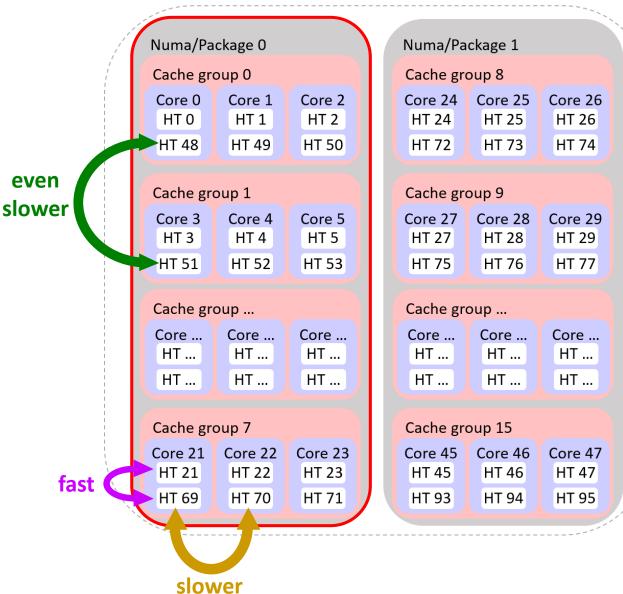
Numa/Pa	ckage 0			Numa/Package 1				
Cache gr	oup 0			Cache gr	Cache group 8			
Core 0 HT 0	Core 1 HT 1	Core 2 HT 2		Core 24 HT 24	Core 25 HT 25	Core 26 HT 26		
HT 48	HT 49	HT 50		HT 72	HT 73	HT 74		
Cache gr	oup 1			Cache group 9				
Core 3 HT 3	Core 4 HT 4	Core 5 HT 5		Core 27 HT 27	Core 28 HT 28	Core 29 HT 29		
HT 51	HT 52	HT 53		HT 75	HT 76	HT 77		
Cache gr	oup			Cache group				
Core HT	Core HT	Core HT		Core HT	Core HT	Core HT		
HT	HT	HT		HT	HT	HT		
Cache gr	oup 7		Cache group 15					
Core 21 HT 21	Core 22 HT 22	Core 23 HT 23		Core 45 HT 45	Core 46 HT 46	Core 47 HT 47		
HT 69	HT 70	HT 71		HT 93	HT 94	HT 95		

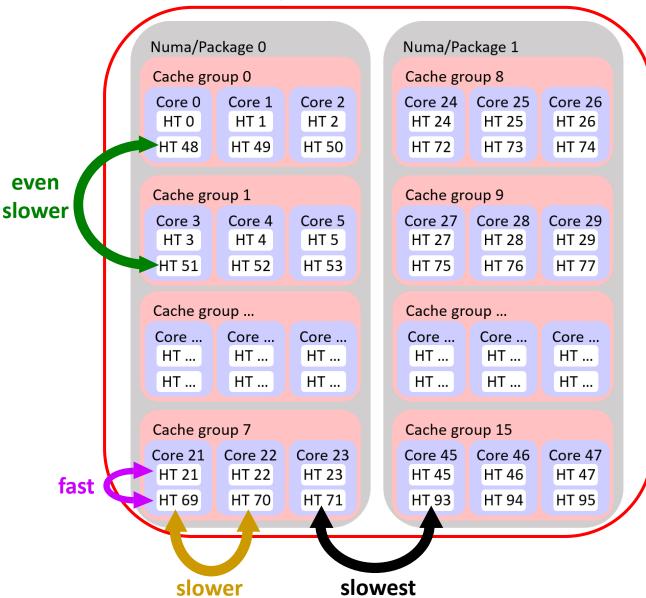
Numa/Pa	ackage 0		Numa/Package 1					
Cache gi	roup 0			Cache group 8				
Core 0 HT 0	Core 1 HT 1	Core 2 HT 2		Core 24 HT 24	Core 25 HT 25	Core 26 HT 26		
HT 48	HT 49	HT 50		HT 72	HT 73	HT 74		
Cache gi	roup 1			Cache group 9				
Core 3 HT 3	Core 4 HT 4	Core 5 HT 5		Core 27 HT 27	Core 28 HT 28	Core 29 HT 29		
HT 51	HT 52	HT 53		HT 75	HT 76	HT 77		
Cache gi	roup			Cache group				
Core HT	Core HT	Core HT		Core HT	Core HT	Core HT		
НТ	HT	НТ		HT	HT	HT		
Cache gi	roup 7			Cache gr	oup 15			
Core 21 HT 21	Core 22 HT 22	Core 23 HT 23		Core 45 HT 45	Core 46 HT 46	Core 47 HT 47		
HT 69	HT 70	HT 71		HT 93	HT 94	HT 95		

	Numa/Pa	ckage 0		Numa/Package 1				
	Cache group 0				Cache group 8			
	Core 0 HT 0	Core 1 HT 1	Core 2 HT 2		Core 24 HT 24	Core 25 HT 25	Core 26 HT 26	
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	Cache gr	oup 1			Cache gro	oup 9		
	Core 3 HT 3	Core 4 HT 4	Core 5 HT 5		Core 27 HT 27	Core 28 HT 28	Core 29 HT 29	
	HT 51	HT 52	HT 53		HT 75	HT 76	HT 77	
	Cache gr	oup			Cache group			
	Core HT	Core HT	Core HT		Core HT	Core HT	Core HT	
	HT	HT	HT		HT	HT	HT	
	Cache group 7					oup 15		
	Core 21 HT 21	Core 22 HT 22	Core 23 HT 23		Core 45 HT 45	Core 46 HT 46	Core 47 HT 47	
fast 🤇	HT 69	HT 70	HT 71		HT 93	HT 94	HT 95	

	Numa/Pa	ckage 0		Numa/Pa	ckage 1			
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	Core 0 HT 0	Core 1 HT 1	Core 2 HT 2		Core 24 HT 24	Core 25 HT 25	Core 26 HT 26	
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	Cache gro	oup 1			Cache gr	oup 9		
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	HT 51	HT 52	HT 53		HT 75	HT 76	HT 77	
	Cache group				Cache group			
	Core HT	Core HT	Core HT		Core HT	Core HT	Core HT	
	HT	HT	HT		HT	HT	HT	
	Cache gro	oup 7			Cache group 15			
fast	Core 21 HT 21	Core 22 HT 22	Core 23 HT 23		Core 45 HT 45	Core 46 HT 46	Core 47 HT 47	
	HT 69	HT 70	HT 71		HT 93	HT 94	HT 95	ļ
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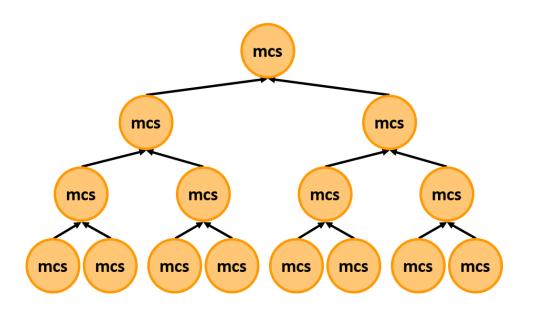
Many-core NUMA system Numa/Package 0 Numa/Package 1 Cache group 0 Cache group 8 Core 25 Core 26 Core 0 Core 1 Core 2 Core 24 HT 0 HT 2 HT 24 HT 25 HT 26 HT 1 HT 73 HT 74 HT 48 HT 49 HT 50 HT 72 even Cache group 1 Cache group 9 slower Core 4 Core 5 Core 27 Core 28 Core 29 Core 3 HT 3 HT 4 HT 5 HT 27 HT 28 HT 29 HT 51 HT 52 HT 53 HT 75 HT 76 HT 77 Cache group ... Cache group ... Core ... Core ... Core ... Core ... Core ... Core ... HT ... Cache group 7 Cache group 15 Core 22 Core 23 Core 45 Core 47 Core 21 Core 46 HT 21 HT 22 HT 23 HT 45 HT 46 HT 47 fast HT 69 HT 70 HT 94 HT 95 HT 71 HT 93

slowest

slower

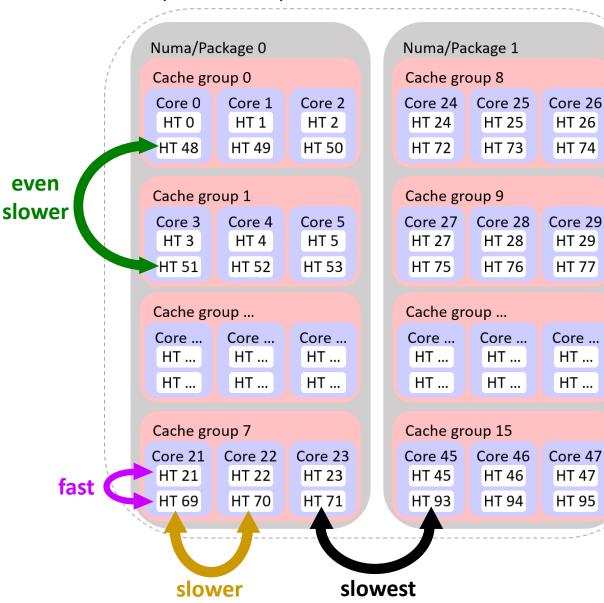
Multi-level NUMA-aware Locks

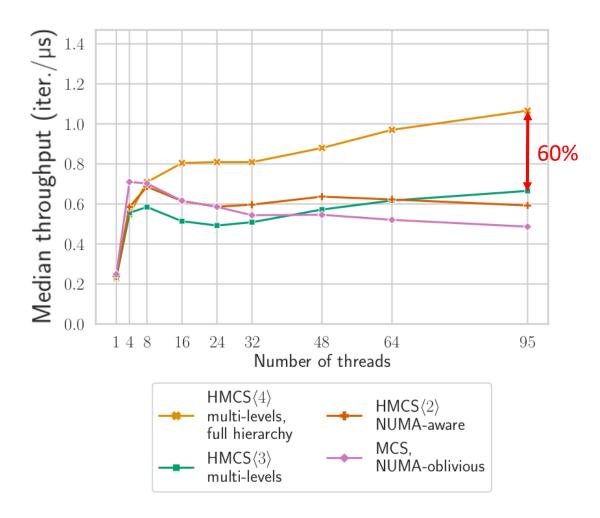
- HMCS creates a hierarchy of MCS locks
 - Arbitrary number of levels



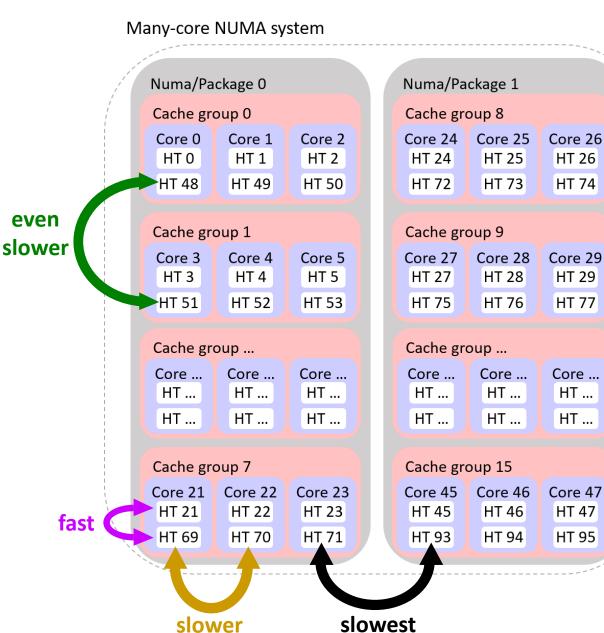
Many-core NUMA system

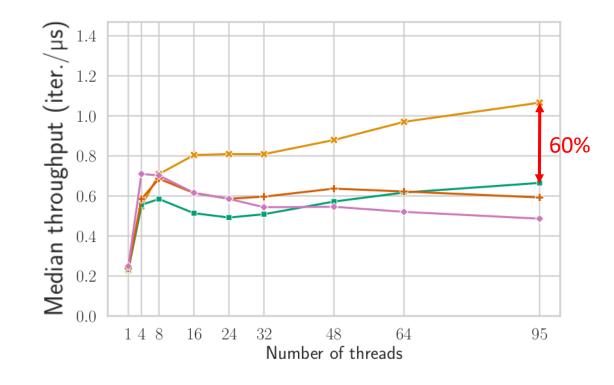
Multi-level NUMA-aware Locks



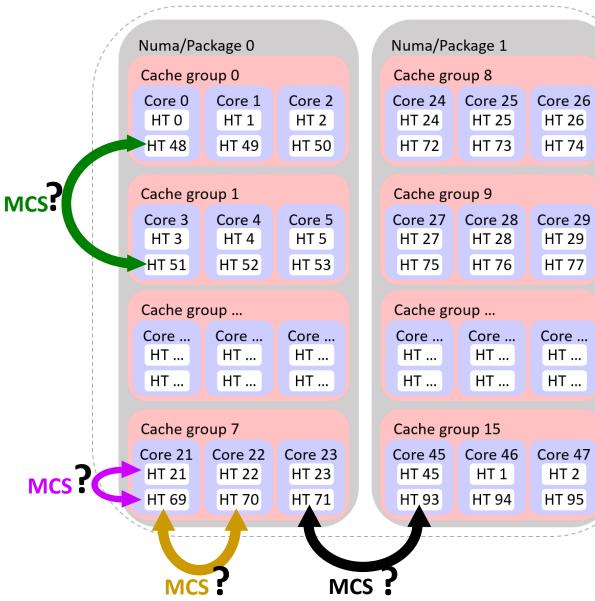


Multi-level NUMA-aware Locks

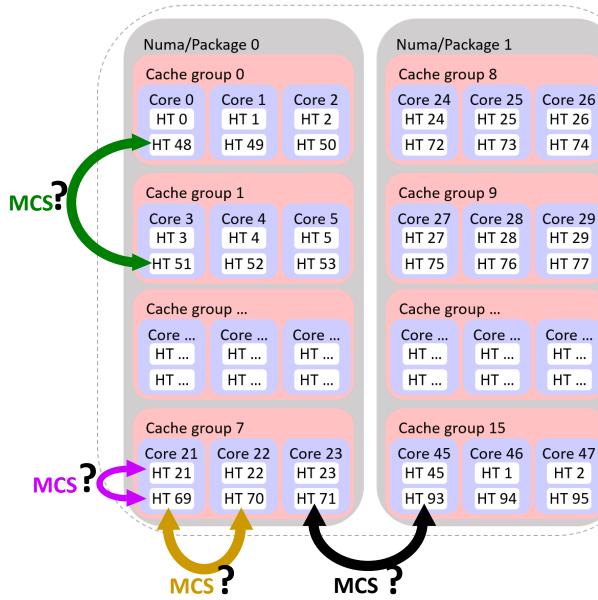




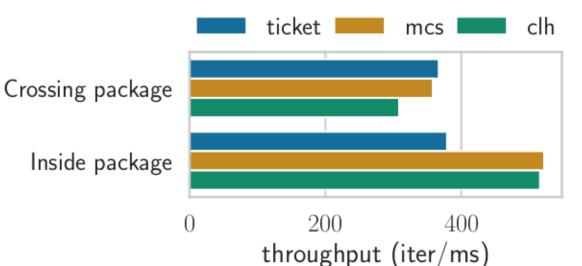
Multi-Level: Utilizing the full deep-hierarchy in a lock improves performance



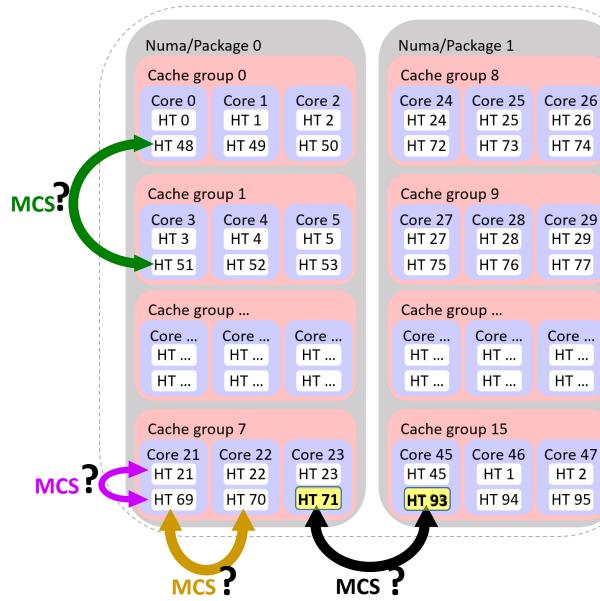
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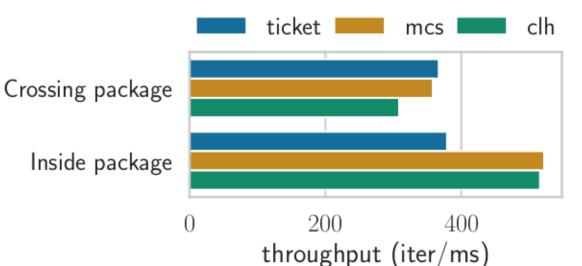
Experiment - Heterogeneity



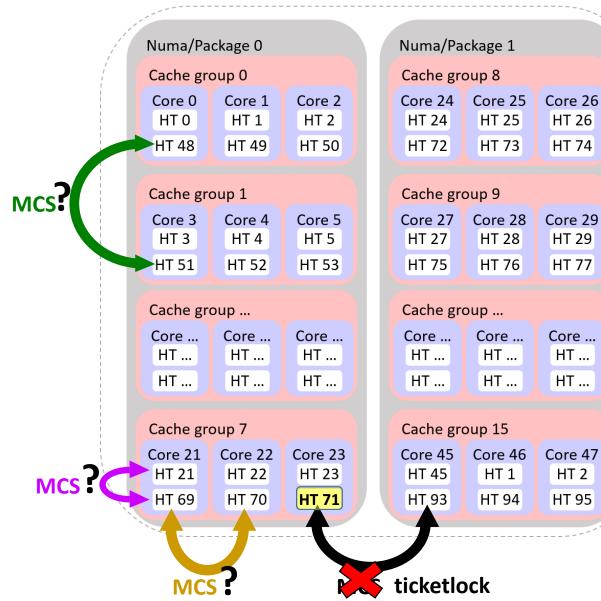
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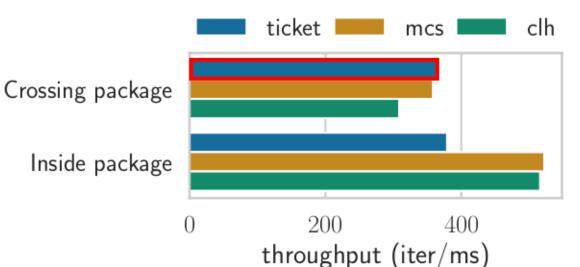
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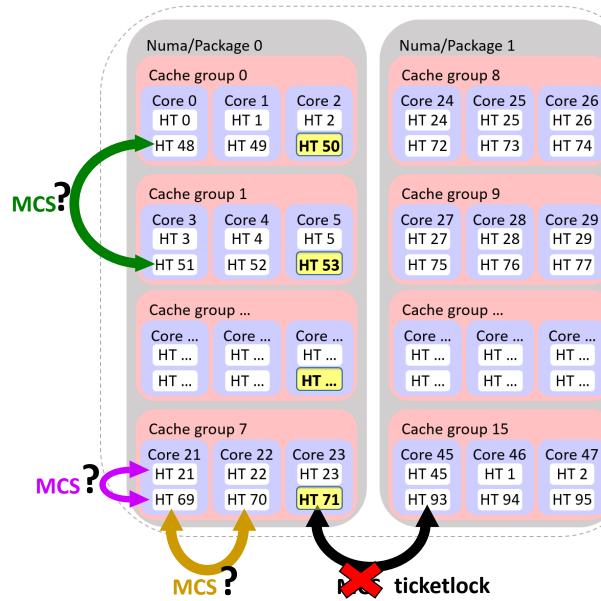
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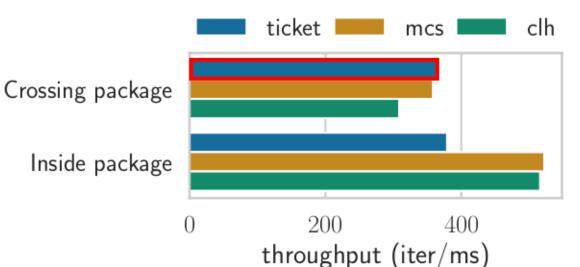
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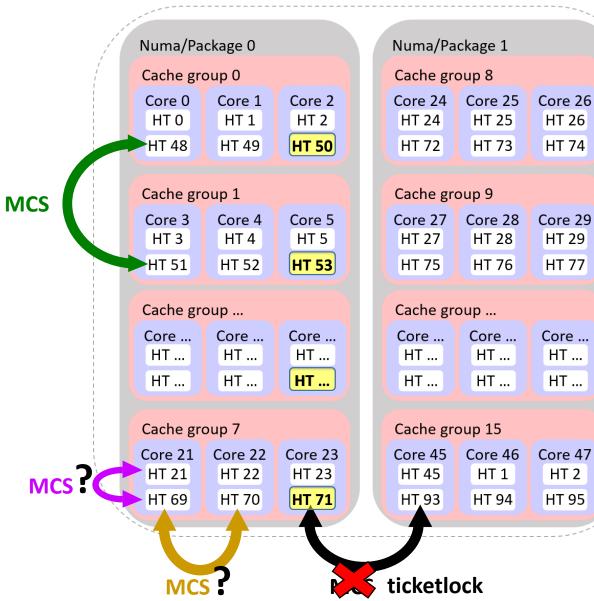
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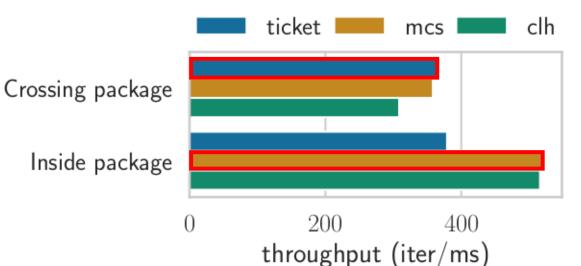
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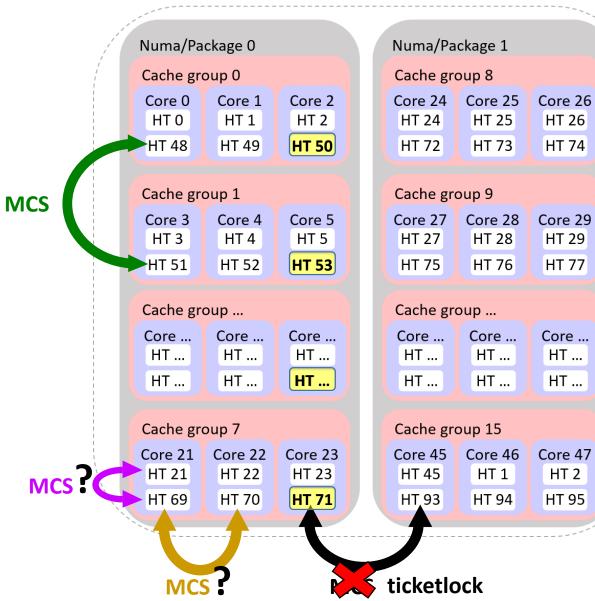
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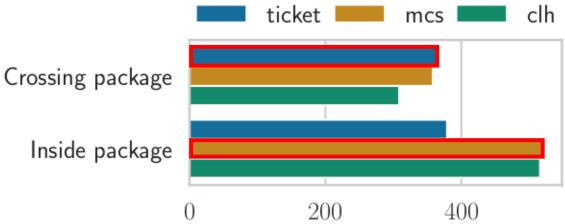


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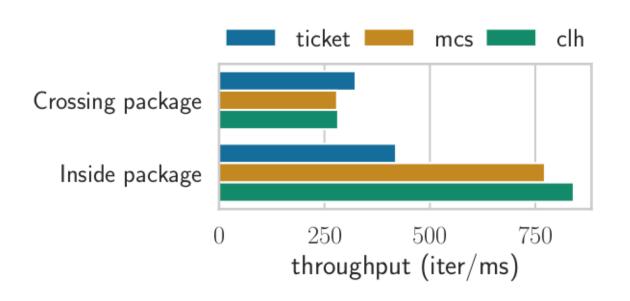


Experiment - Heterogeneity

x86 server – execution of classical locks in isolation

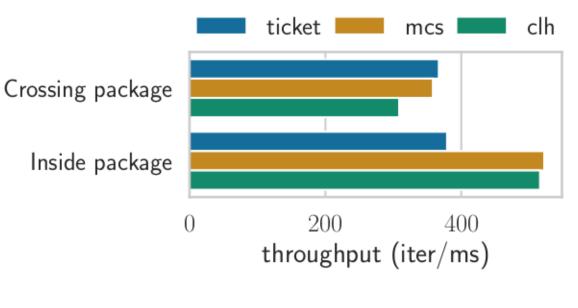


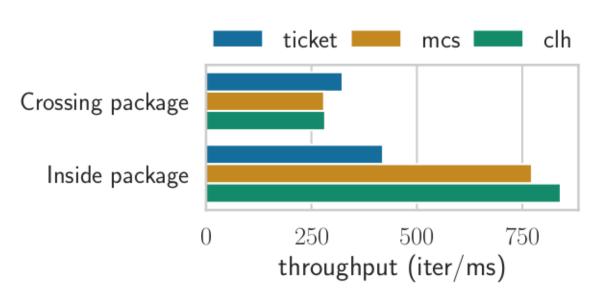
throughput (iter/ms)



Arm server – execution of classical locks in isolation

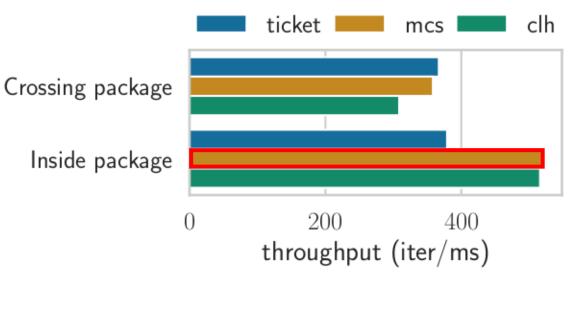
x86 server – execution of classical locks in isolation

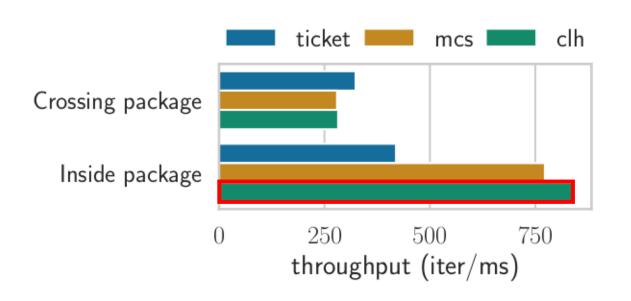




Arm server – execution of classical locks in isolation

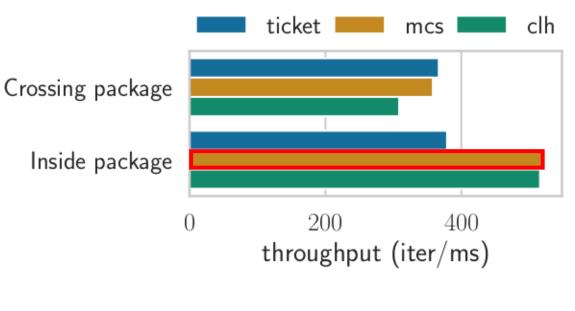
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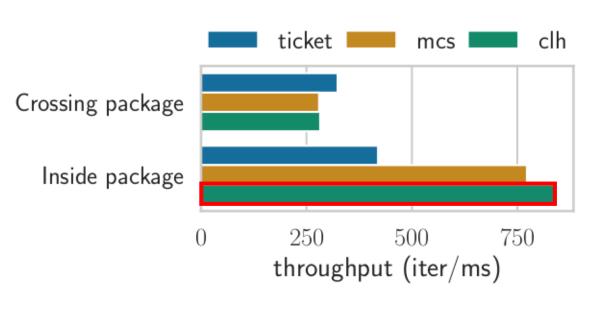




Arm server – execution of classical locks in isolation

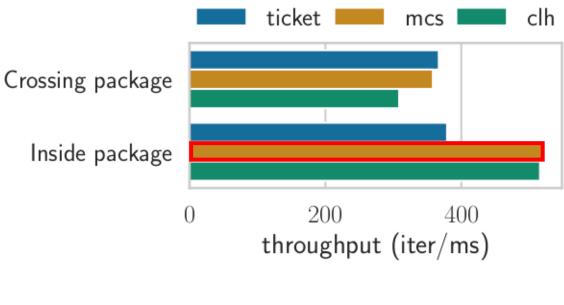
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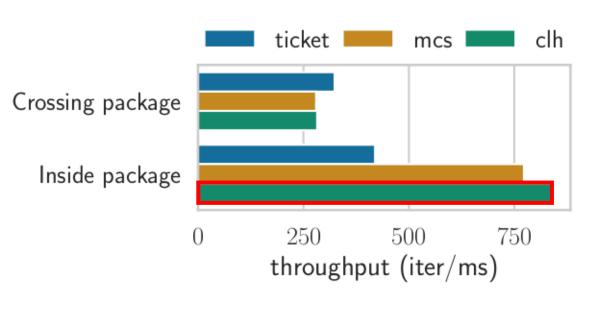




Arm server – execution of classical locks in isolation

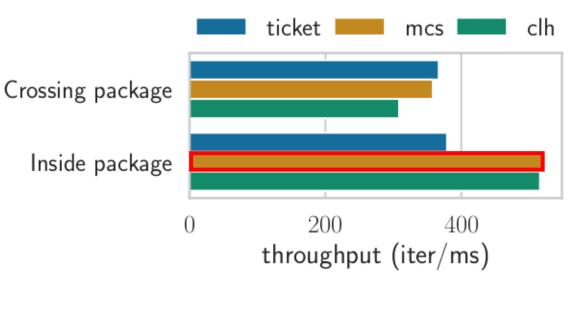
Platform Optimization: For different platforms, the best lock for a level may differ x86 server – execution of classical locks in isolation





Arm server – execution of classical locks in isolation

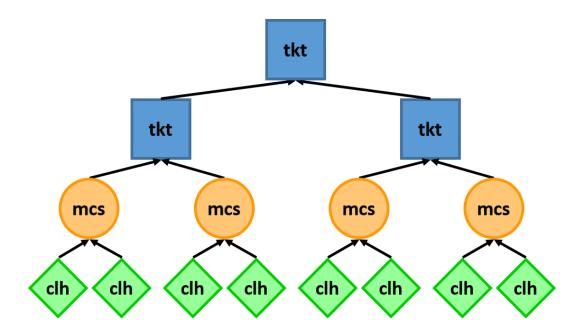
Platform Optimization: For different platforms, the best lock for a level may differ x86 server – execution of classical locks in isolation



Level-heterogeneity: For different levels, the best lock may differ

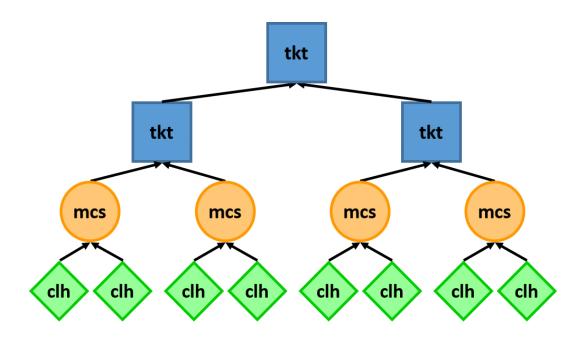
So, how does this affects our lock design?

Our Desired NUMA-aware lock



- Multi-Level
- Level-Heterogeneous
- Configurability for Platform Optimization

Our Desired NUMA-aware lock



- Multi-Level
- Level-Heterogeneous
- Configurability for Platform Optimization

• Showing lock correctness is

challenging

• Weak Memory Models (WMMs) make it even more complicated

Our contribution: CLoF

We propose CLoF, a framework to generate locks for a target platform:

- that support an arbitrary hierarchy;
- for each level, the lock implementation may be different;
- that are *correct-by-construction* on Weak Memory Models.

Our contribution: CLoF

We propose CLoF, a framework to generate locks for a target platform:

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NUMA-aware locks		Correctness on WMMs	Level heterogeneity & Architecture optimization	Multi-Level
lock cohorting	PPPoPP'12	×	\checkmark	×
HMCS	PPoPP'15	x 1	×	\checkmark
CNA lock	EuroSys'19	×	×	×
ShflLock	SOSP'19	×	×	×
CLoF	SOSP'21	\checkmark	\checkmark	\checkmark

CLoF Workflow

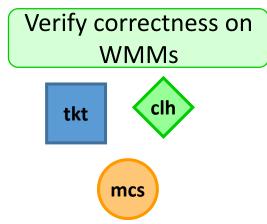
Discover Memory Hierarchy

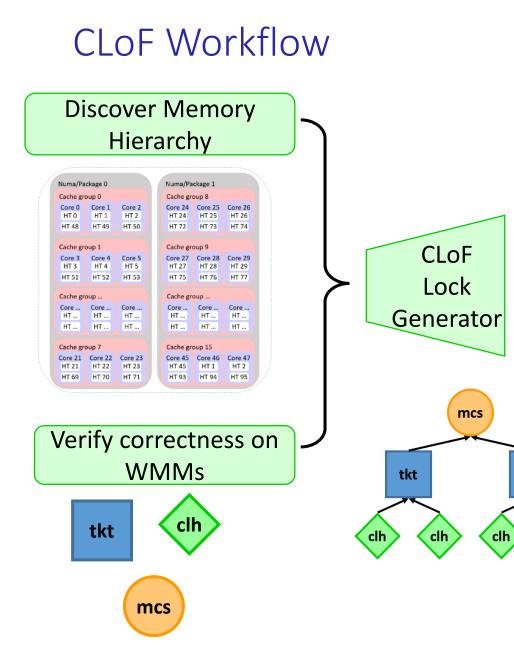
Í	Numa/Pa	ickage 0		Numa/Package 1			
	Cache gr	oup 0		Cache group 8			
	Core 0 HT 0	Core 1 HT 1	Core 2 HT 2	Core 24 HT 24	Core 25 HT 25	Core 26 HT 26	
	HT 48	HT 49	HT 50	HT 72	HT 73	HT 74	
	Cache gr	oup 1		Cache gr	oup 9		
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	HT 51	HT 52	HT 53	HT 75	HT 76	HT 77	
	Cache gr	oup		Cache gr	oup		
	Core HT	Core HT	Core HT	Core HT	Core HT	Core HT	
	HT	HT	HT	HT	HT	HT	
	Cache gr	-		Cache gr	-		
	Core 21 HT 21	Core 22 HT 22	Core 23 HT 23	Core 45 HT 45	Core 46 HT 1	Core 47 HT 2	
ς,	HT 69	HT 70	HT 71	HT 93	HT 94	HT 95	

CLoF Workflow

Discover Memory Hierarchy

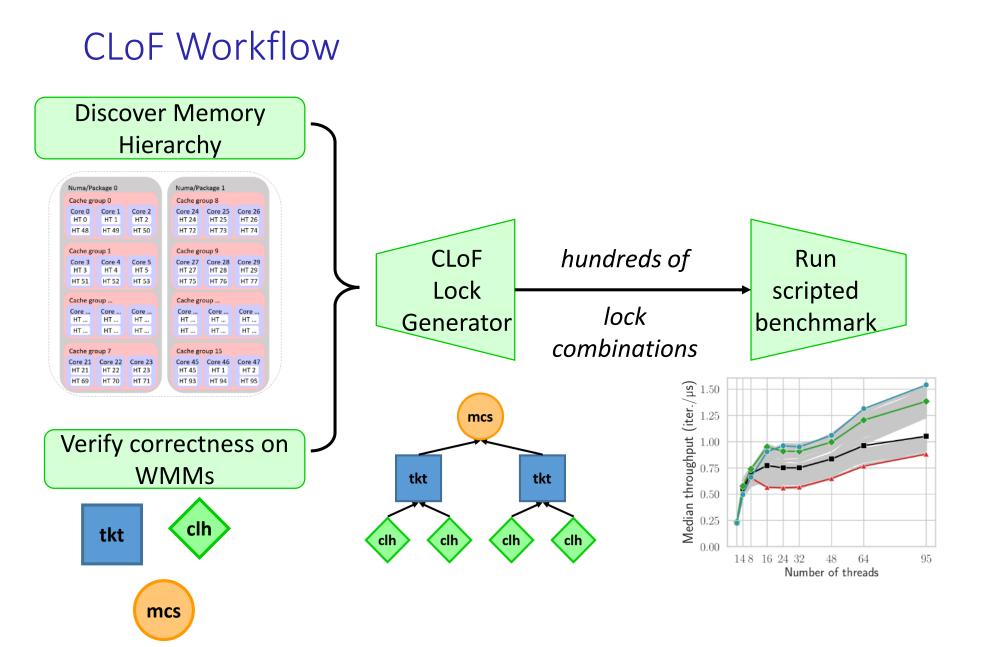
1	Numa/Pa	ickage 0		Numa/Pa	ickage 1	
	Cache gr	oup 0		Cache gr	oup 8	
	Core 0 HT 0	Core 1 HT 1	Core 2 HT 2	Core 24 HT 24	Core 25 HT 25	Core 26 HT 26
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	Cache gr	oup		Cache gr	oup	
	Core HT	Core HT	Core HT	Core HT	Core HT	Core HT
	HT	HT	HT	HT	HT	HT
	Cache gr	oup 7		Cache gr	oup 15	
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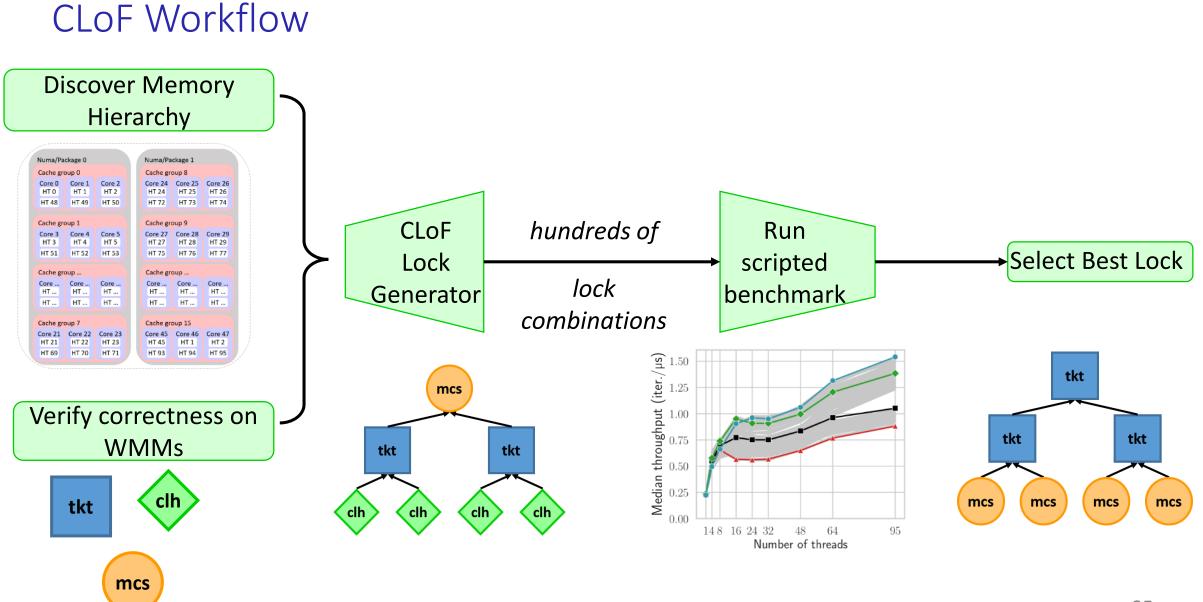




tkt

clh







- How to figure out the hierarchy we need to use?
- How does our CLoF Lock Generator works?
- How do we know it is correct?
- How do we pick the best lock for the target platform?



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- How does our CLoF Lock Generator works?
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- How do we pick the best lock for the target platform?

Operating systems know the hierarchy

• Visible with Linux's lscpu and lstopo

Package ()			Package 2	L		
NUMAC)			NUMA 2			
Core 0	Core 1	Core 4	Core 6	Core 64	Core 65	Core 68	Core 69
Core 2	Core 3	Core 5	Core 7	Core 66	Core 67	Core 70	Core 71
Core	Core	Core 28	Core 29	Core	Core	Core 92	Core 93
Core	Core	Core 30	Core 31	Core	Core	Core 94	Core 95
NUMA 1				NUMA 3	i		
Core 32	Core 33	Core 36	Core 37	Core 96	Core 97	Core 100	Core 101
Core 34	Core 35	Core 38	Core 39	Core 98	Core 99	Core 102	Core 103
Core	Core	Core 60	Core 61	Core	Core	Core 124	Core 125
C	Core	Core 62	Core 63	Core	Core	Core 126	Core 127
Core							

Taishan 200 server – Armv8

Operating systems know the hierarchy

• Visible with Linux's lscpu and lstopo

Package 0 Package 1 NUMA 0 NUMA 2 Core 0 Core 1 Core 4 Core 6 Core 65 Core 68 Core 69 Core 2 Core 3 Core 5 Core 7 Core 66 Core 67 Core 92 Core 93 Core Core Core 30 Core 31 Core 92 Core 93 NUMA 1 Core 32 Core 33 Core 36 Core 37 Core 97 Core 100 Core 101 Core Core Core 60 Core 61 Core Core Core 102 Core 103 Core Core Core 60 Core 61 Core Core Core 124 Core 125 Core Core Core 62 Core 63 Core Core Core 126 Core 125										
Core 0Core 1Core 4Core 6Core 64Core 65Core 68Core 69Core 2Core 3Core 5Core 7Core 66Core 67Core 70Core 71CoreCoreCore 28Core 29CoreCoreCore 92Core 93CoreCoreCore 30Core 31CoreCoreCore 94Core 95NUMA 1NUMA 3Core 32Core 33Core 36Core 37Core 96Core 97Core 100Core 101CoreCore 60Core 61CoreCoreCore 124Core 125	Pad	ckage C)				Package 1	L		
Core 2 Core 3 Core 5 Core 7 Core 66 Core 67 Core 70 Core 71 Core Core Core 28 Core 29 Core Core Core 92 Core 93 Core Core Core 30 Core 31 Core Core Core 92 Core 93 NUMA 1 NUMA 3 NUMA 3 Core 33 Core 36 Core 37 Core 96 Core 97 Core 100 Core 101 Core Core Core 60 Core 61 Core Core Core 124 Core 125	N	UMA 0					NUMA 2			
CoreCore 28Core 29Core 29Core 93CoreCoreCoreCoreCore 93Core 93CoreCoreCoreCoreCore 94Core 95NUMA 1NUMA 3NUMA 3Core 32Core 33Core 36Core 37Core 96Core 97Core 100Core 101CoreCoreCore 60Core 61CoreCoreCore 124Core 125	C	ore 0	Core 1	Core 4	Core 6		Core 64	Core 65	Core 68	Core 69
Core Core 30 Core 31 Core Core Core 94 Core 95 NUMA 1 NUMA 3 NUMA 3 NUMA 3 Core 32 Core 33 Core 36 Core 37 Core 96 Core 97 Core 100 Core 101 Core Core Core Core Core 102 Core 103 Core Core Core Core Core 124 Core 125	C	ore 2	Core 3	Core 5	Core 7		Core 66	Core 67	Core 70	Core 71
Core Core 30 Core 31 Core Core Core 94 Core 95 NUMA 1 NUMA 3 NUMA 3 NUMA 3 Core 32 Core 33 Core 36 Core 37 Core 96 Core 97 Core 100 Core 101 Core Core Core 60 Core 61 Core Core Core 124 Core 125										
NUMA 1 NUMA 3 Core 32 Core 33 Core 36 Core 37 Core 38 Core 39 Core 96 Core 97 Core 100 Core 101 Core 102 Core 103 Core Core Core 60 Core 61 Core Core Core 124 Core 125	C	ore	Core	Core 28	Core 29		Core	Core	Core 92	Core 93
Core 32Core 33Core 36Core 37Core 96Core 97Core 100Core 101Core 34Core 35Core 38Core 39Core 98Core 99Core 102Core 103CoreCoreCore 60Core 61CoreCoreCore 124Core 125	C	ore	Core	Core 30	Core 31		Core	Core	Core 94	Core 95
Core 34 Core 35 Core 38 Core 39 Core 98 Core 99 Core 102 Core 103 Core Core Core Core Core 124 Core 125	N	UMA 1					NUMA 3			
Core Core 60 Core 61 Core Core Core 124 Core 125	Сс	ore 32	Core 33	Core 36	Core 37		Core 96	Core 97	Core 100	Core 101
	Co	ore 34	Core 35	Core 38	Core 39		Core 98	Core 99	Core 102	Core 103
Core Core 62 Core 63 Core Core 126 Core 127	C	ore	Core	Core 60	Core 61		Core	Core	Core 124	Core 125
	C	ore	Core	Core 62	Core 63		Core	Core	Core 126	Core 127

Taishan 200 server – Armv8

Is this the **full** hierarchy?

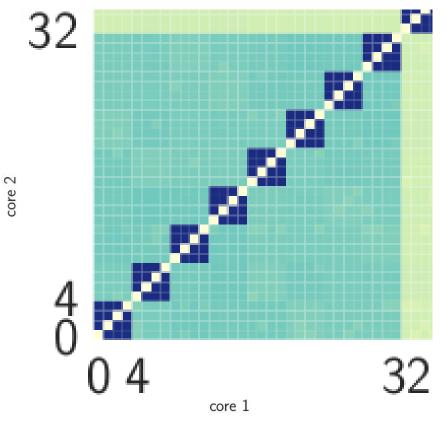
Operating systems know the hierarchy

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,i'	Package (D				Package 2	1			
	NUMA ()				NUMA 2	!			
	Core 0	Core 1	Core 4	Core 6		Core 64	Core 65	Core 68	Core 69	
	Core 2	Core 3	Core 5	Core 7		Core 66	Core 67	Core 70	Core 71	
	Core	Core	Core 28	Core 29		Core	Core	Core 92	Core 93	
	Core	Core	Core 30	Core 31		Core	Core	Core 94	Core 95	
	NUMA 1					NUMA 3	;			
	Core 32	Core 33	Core 36	Core 37		Core 96	Core 97	Core 100	Core 101	
	Core 34	Core 35	Core 38	Core 39		Core 98	Core 99	Core 102	Core 103	
	Core	Core	Core 60	Core 61		Core	Core	Core 124	Core 125	
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Taishan 200 server – Armv8

- 2 threads alternately increment a shared counter
- Darker colors => Higher throughput



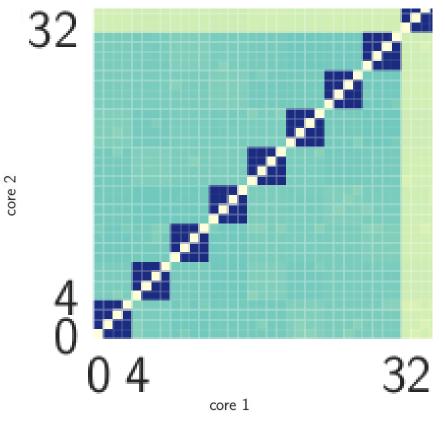
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Packa	ge 0	1			Package 2	1			
NUM	IA 0				NUMA 2	!			
Core	0	Core 1	Core 4	Core 6	Core 64	Core 65	Core 68	Core 69	
Core	2	Core 3	Core 5	Core 7	Core 66	Core 67	Core 70	Core 71	
Core		Core	Core 28	Core 29	Core	Core	Core 92	Core 93	
Core		Core	Core 30	Core 31	Core	Core	Core 94	Core 95	
NUM	IA 1				NUMA 3	;			
Core	32	Core 33	Core 36	Core 37	Core 96	Core 97	Core 100	Core 101	
Core	34	Core 35	Core 38	Core 39	Core 98	Core 99	Core 102	Core 103	
Core		Core	Core 60	Core 61	Core	Core	Core 124	Core 125	
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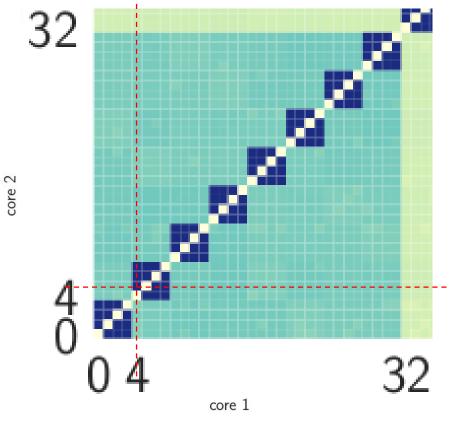
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	Core 2	Core 3	Core 5	Core 7	Core 66	Core 67	Core 70	Core 71	
	Core	Core	Core 28	Core 29	Core	Core	Core 92	Core 93	
	Core	Core	Core 30	Core 31	Core	Core	Core 94	Core 95	
	NUMA 1				NUMA 3				
	Core 32	Core 33	Core 36	Core 37	Core 96	Core 97	Core 100	Core 101	
	Core 34	Core 35	Core 38	Core 39	Core 98	Core 99	Core 102	Core 103	
	Core	Core	Core 60	Core 61	Core	Core	Core 124	Core 125	
	Core	Core	Core 62	Core 63	Core	Core	Core 126	Core 127	
									1
									~

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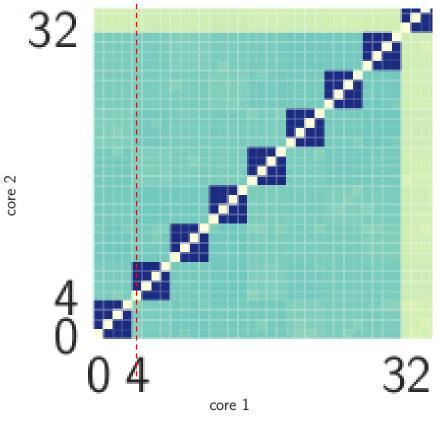
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, í ⁻	Package ()			Package 1	L			
	NUMA 0)			NUMA 2				
	Core 0	Core 1	Core 4	Core 6	Core 64	Core 65	Core 68	Core 69	
	Core 2	Core 3	Core 5	Core 7	Core 66	Core 67	Core 70	Core 71	
	Core	Core	Core 28	Core 29	Core	Core	Core 92	Core 93	
	Core	Core	Core 30	Core 31	Core	Core	Core 94	Core 95	
	NUMA 1				NUMA 3				
	Core 32	Core 33	Core 36	Core 37	Core 96	Core 97	Core 100	Core 101	
	Core 34	Core 35	Core 38	Core 39	Core 98	Core 99	Core 102	Core 103	
	Core	Core	Core 60	Core 61	Core	Core	Core 124	Core 125	
	Core	Core	Core 62	Core 63	Core	Core	Core 126	Core 127	
									1
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Taishan 200 server – Armv8

- 2 threads alternately increment a shared counter
- Darker colors => Higher throughput



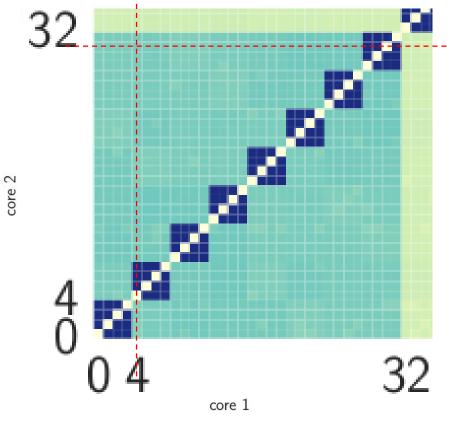
Operating systems know the hierarchy

• Visible with Linux's lscpu and lstopo

, í ⁻	Package ()			Package 1	L			
	NUMA 0)			NUMA 2				
	Core 0	Core 1	Core 4	Core 6	Core 64	Core 65	Core 68	Core 69	
	Core 2	Core 3	Core 5	Core 7	Core 66	Core 67	Core 70	Core 71	
	Core	Core	Core 28	Core 29	Core	Core	Core 92	Core 93	
	Core	Core	Core 30	Core 31	Core	Core	Core 94	Core 95	
	NUMA 1				NUMA 3				
	Core 32	Core 33	Core 36	Core 37	Core 96	Core 97	Core 100	Core 101	
	Core 34	Core 35	Core 38	Core 39	Core 98	Core 99	Core 102	Core 103	
	Core	Core	Core 60	Core 61	Core	Core	Core 124	Core 125	
	Core	Core	Core 62	Core 63	Core	Core	Core 126	Core 127	
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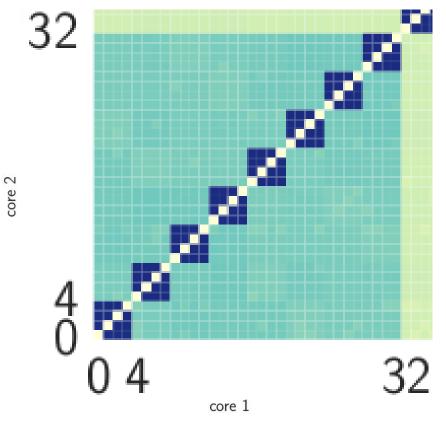
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,i'	Package (D				Package 2	1			
	NUMA ()				NUMA 2	!			
	Core 0	Core 1	Core 4	Core 6		Core 64	Core 65	Core 68	Core 69	
	Core 2	Core 3	Core 5	Core 7		Core 66	Core 67	Core 70	Core 71	
	Core	Core	Core 28	Core 29		Core	Core	Core 92	Core 93	
	Core	Core	Core 30	Core 31		Core	Core	Core 94	Core 95	
	NUMA 1					NUMA 3	;			
	Core 32	Core 33	Core 36	Core 37		Core 96	Core 97	Core 100	Core 101	
	Core 34	Core 35	Core 38	Core 39		Core 98	Core 99	Core 102	Core 103	
	Core	Core	Core 60	Core 61		Core	Core	Core 124	Core 125	
	Core	Core	Core 62	Core 63		Core	Core	Core 126	Core 127	

Taishan 200 server – Armv8

- 2 threads alternately increment a shared counter
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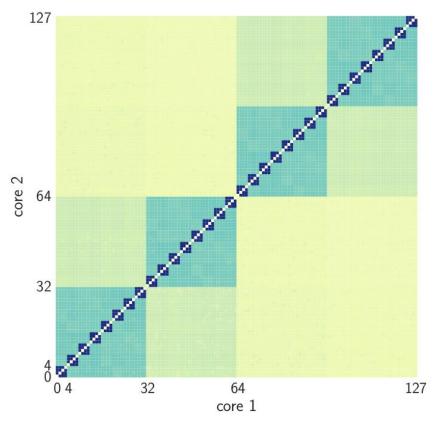
Operating systems know the hierarchy

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Package (C			Package 2	L		
NUMA ()			NUMA 2			
Core 0	Core 1	Core 4	Core 6	Core 64	Core 65	Core 68	Core 69
Core 2	Core 3	Core 5	Core 7	Core 66	Core 67	Core 70	Core 71
Core	Core	Core 28	Core 29	Core	Core	Core 92	Core 93
Core	Core	Core 30	Core 31	Core	Core	Core 94	Core 95
NUMA 1				NUMA 3			
Core 32	Core 33	Core 36	Core 37	Core 96	Core 97	Core 100	Core 101
Core 34	Core 35	Core 38	Core 39	Core 98	Core 99	Core 102	Core 103
Core	Core	Core 60	Core 61	Core	Core	Core 124	Core 125
		C C2	Cama 62	Core	Core	Core 126	Core 127
Core	Core	Core 62	Core 65	core		COIC 120	COTC 12/

Taishan 200 server – Armv8

- 2 threads alternately increment a shared counter
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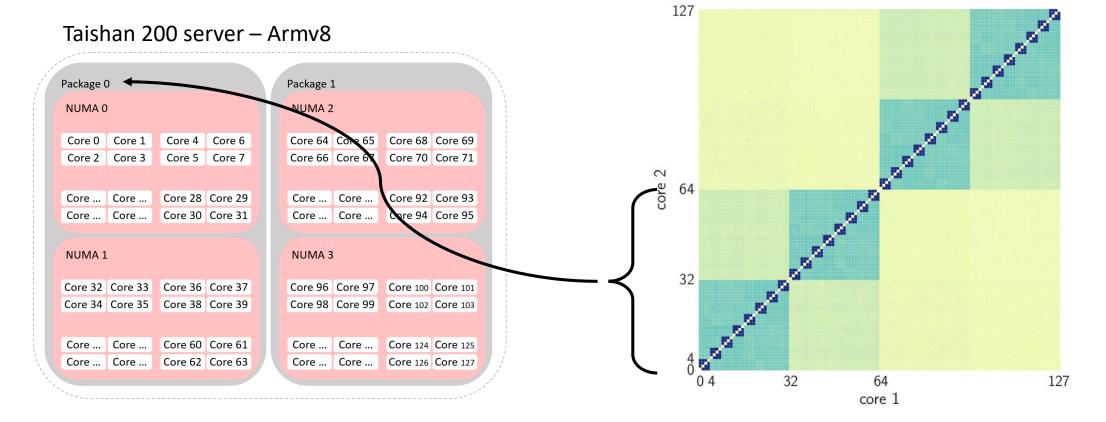


Operating systems know the hierarchy

• Visible with Linux's lscpu and lstopo

Experimental Discovery

- 2 threads alternately increment a shared counter
- Darker colors => Higher throughput



47

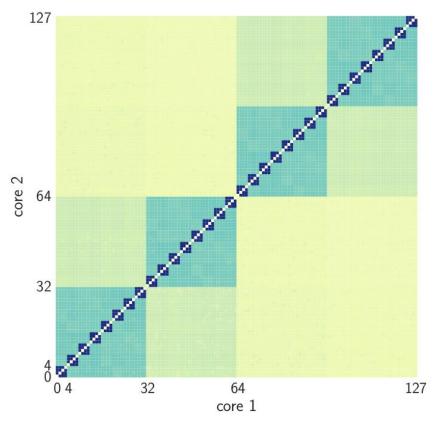
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Package (C			Package 2	L		
NUMA ()			NUMA 2			
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Core	Core	Core 28	Core 29	Core	Core	Core 92	Core 93
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Core	Core	Core 60	Core 61	Core	Core	Core 124	Core 125
		C C2	Cama 62	Core	Core	Core 126	Core 127
Core	Core	Core 62	Core 65	core		COIC 120	COTC 12/

Taishan 200 server – Armv8

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Operating systems know the hierarchy

• Visible with Linux's lscpu and lstopo

Package 0 Package 1 NUMA 2 NUMA 0 Core 64 Core 65 Core 4 Core 6 Core 68 Core 69 Core 0 Core 1 Core 2 Core 3 Core 5 Core 7 Core 66 Core 67 Core 70 Core 71 core 2 64 Core ... Core . Core 92 Core 93 Core ... Core ... Core 28 Core 29 Core 30 Core 31 Core ... Core .. Core 94 Core 95 Core ... Core ... NUMA 1 NUMA 3 32 Core 96 Core 97 Core 32 Core 33 Core 36 Core 37 Core 100 **Sore** 101 Core 102 Core 1 Core 34 Core 35 Core 38 Core 39 Core 98 Core 99 Core 124 Core 125 Core ... Core ... Core 60 Core 61 Core ... Core ... Core 62 Core 63 Core ... Core ... Core 126 Core 127 Core ... Core ... 32 64 127 04 core 1

127

Taishan 200 server – Armv8

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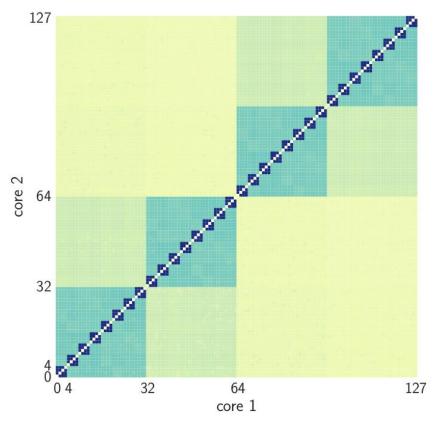
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NUMA 1				NUMA 3			
Core 32	Core 33	Core 36	Core 37	Core 96	Core 97	Core 100	Core 101
Core 34	Core 35	Core 38	Core 39	Core 98	Core 99	Core 102	Core 103
Core	Core	Core 60	Core 61	Core	Core	Core 124	Core 125
		C C2	Cama 62	Core	Core	Core 126	Core 127
Core	Core	Core 62	Core 65	core		COTC 120	COTC 12/

Taishan 200 server – Armv8

- 2 threads alternately increment a shared counter
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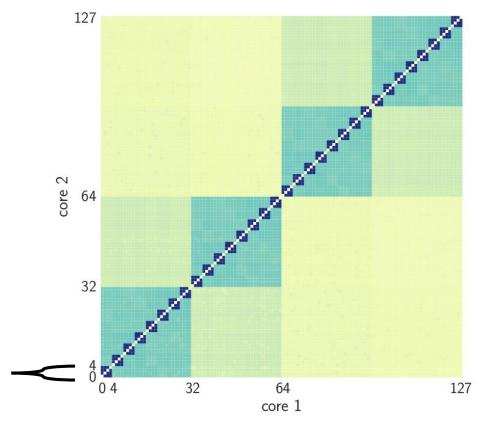
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ackage ()			Package 1	1		
NUMA ()			NUMA 2	!		
Core 0	Core 1	Core 4	Core 6	Core 64	Core 65	Core 68	Core 69
Core 2	Core 3	Core 5	Core 7	Core 66	Core 67	Core 70	Core 71
Core	Core	Core 28	Core 29	Core	Core	Core 92	Core 93
Core	Core	Core 30	Core 31	Core	Core	Core 94	Core 95
NUMA 1				NUMA 3	5		
Core 32	Core 33	Core 36	Core 37	Core 96	Core 97	Core 100	Core 101
	Core 35	Core 38	Core 39	Core 98	Core 99	Core 102	Core 103
Core 34							
Core 34				Core	Core	Core 124	Core 125
Core 34 Core	Core	Core 60	Core 61	core			

Taishan 200 server – Armv8

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Operating systems know the hierarchy

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, ^{, , ,}	Package 0					Package 1 NUMA 2				
	NUMA 0									
	Core 0	Core 1	Core 4	Core 6		Core 64	Core 65	Core 68	Core 69	
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	Core	Core	Core 28	Core 29		Core	Core	Core 92	Core 93	
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	Core 34	Core 35	Core 38	Core 39		Core 98	Core 99	Core 102	Core 103	
	Core	Core	Core 60	Core 61		Core	Core	Core 124	Core 125	
	Core	Core	Core 62	Core 63		Core	Core	Core 126	Core 127	
										/

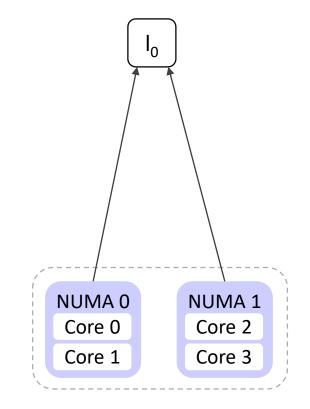
Taishan 200 server – Armv8

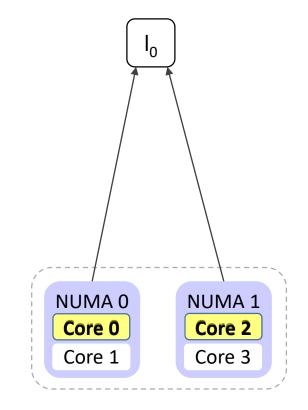
- Not shown by lscpu/lstopo
- Information is shown in processors' datasheet
 - Not efficient
 - Remained unstudied and unused
 - HMCS<4> includes hidden

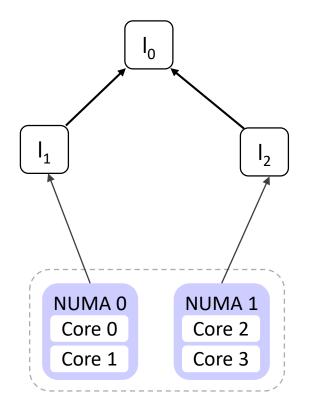
cache group level

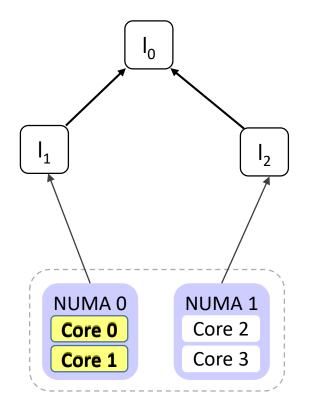


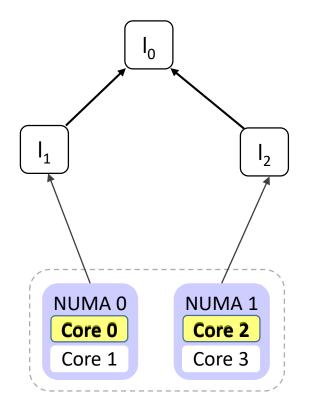
- How to figure out the hierarchy we need to use?
- How does our CLoF Lock Generator works?
- How do we know it is correct?
- How do we pick the best lock for the target platform?



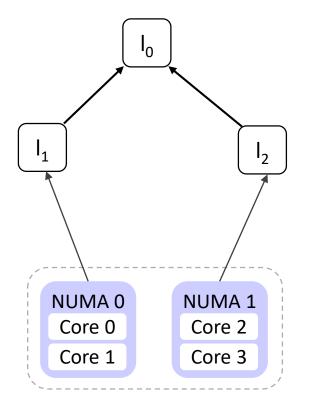






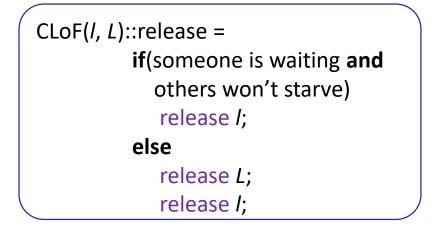


Two NUMA node example

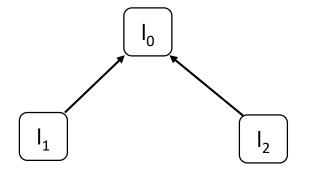


Simplified Code

CLoF(*I*, *L*)::acquire = acquire *I*; if(¬already has *L*) acquire *L*;



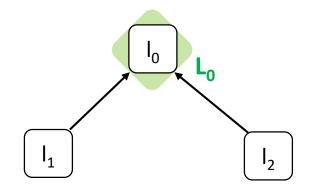
Compile-Time Syntactic Recursion



Simplified Code

CLoF(*I*, *L*)::acquire = acquire *I*; if(¬already has *L*) acquire *L*;

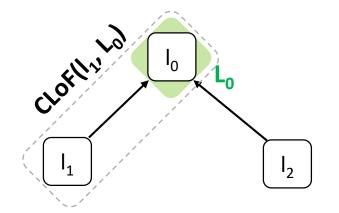
Compile-Time Syntactic Recursion



Simplified Code

CLoF(*I*, *L*)::acquire = acquire *I*; if(¬already has *L*) acquire *L*;

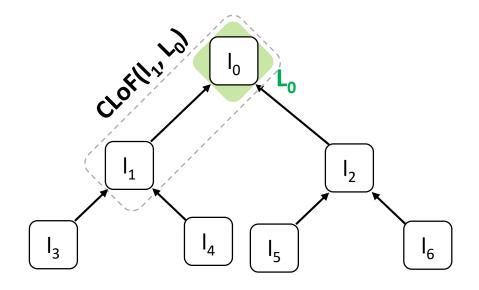
Compile-Time Syntactic Recursion



Simplified Code

CLoF(*I*, *L*)::acquire = acquire *I*; if(¬already has *L*) acquire *L*;

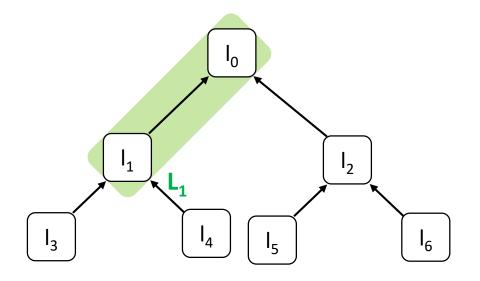
Compile-Time Syntactic Recursion



Simplified Code

CLoF(*I*, *L*)::acquire = acquire *I*; if(¬already has *L*) acquire *L*;

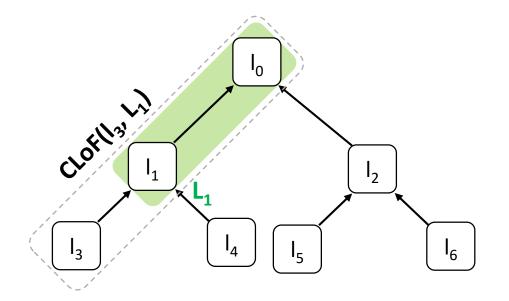
Compile-Time Syntactic Recursion



Simplified Code

CLoF(*I*, *L*)::acquire = acquire *I*; if(¬already has *L*) acquire *L*;

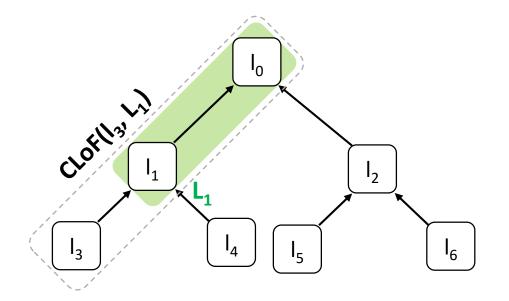
Compile-Time Syntactic Recursion



Simplified Code

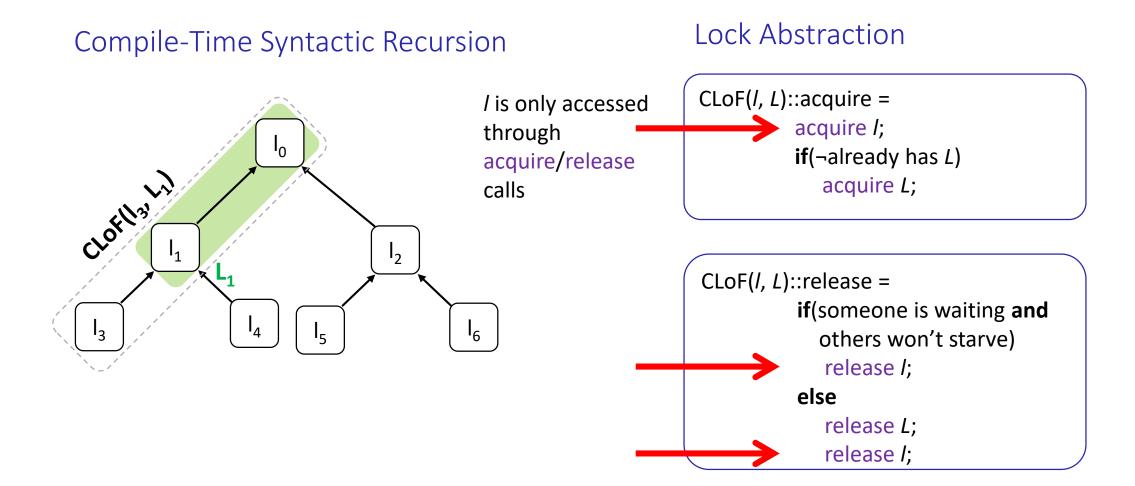
CLoF(*I*, *L*)::acquire = acquire *I*; if(¬already has *L*) acquire *L*;

Compile-Time Syntactic Recursion



Lock Abstraction

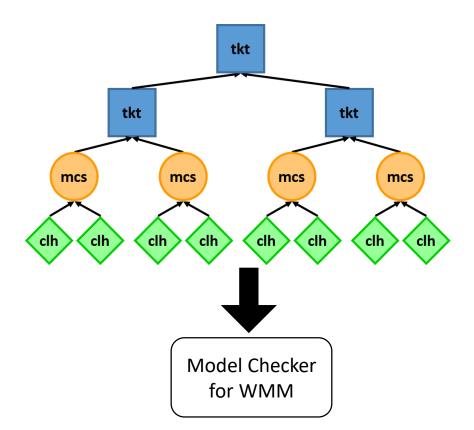
CLoF(*I*, *L*)::acquire = acquire *I*; if(¬already has *L*) acquire *L*;



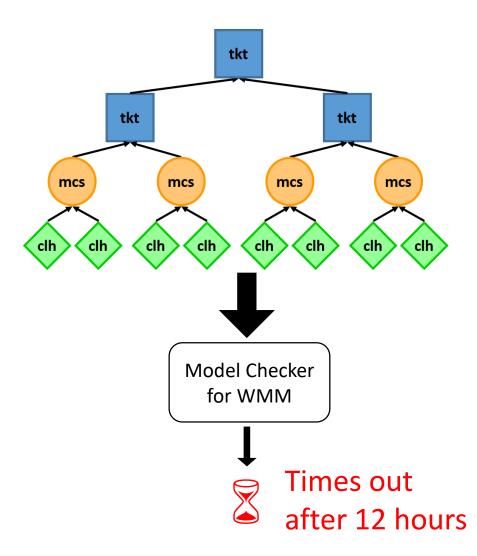


- How to figure out the hierarchy we need to use?
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- How do we know it is correct?
- How do we pick the best lock for the target platform?

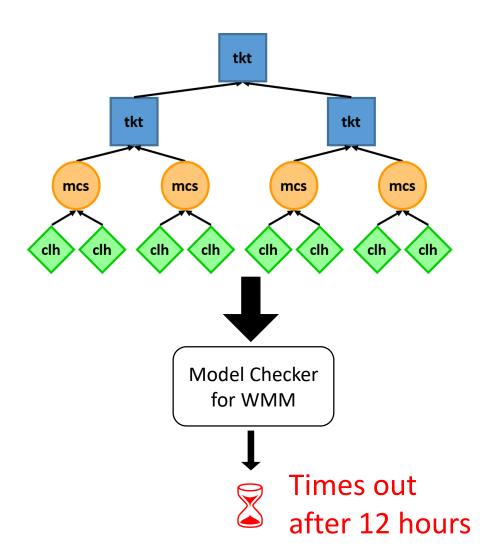
CLoF Correctness



CLoF Correctness



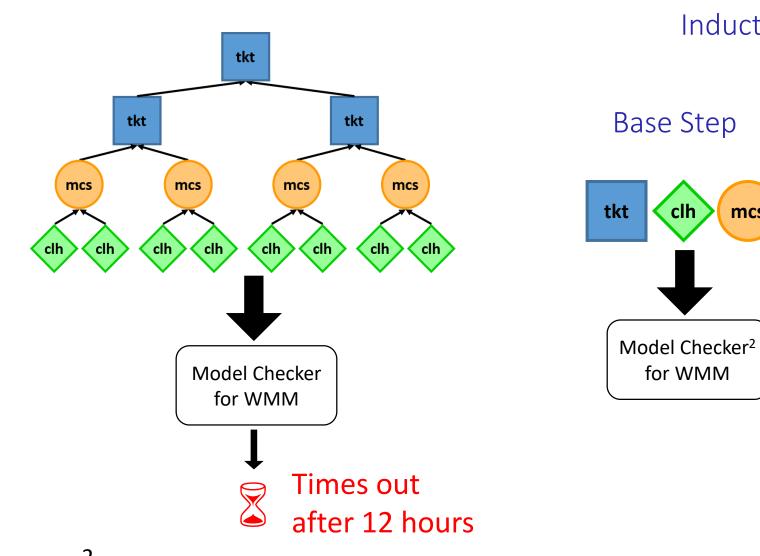
CLoF Correctness



Inductive Approach

Base Step

Inductive Step



Inductive Approach

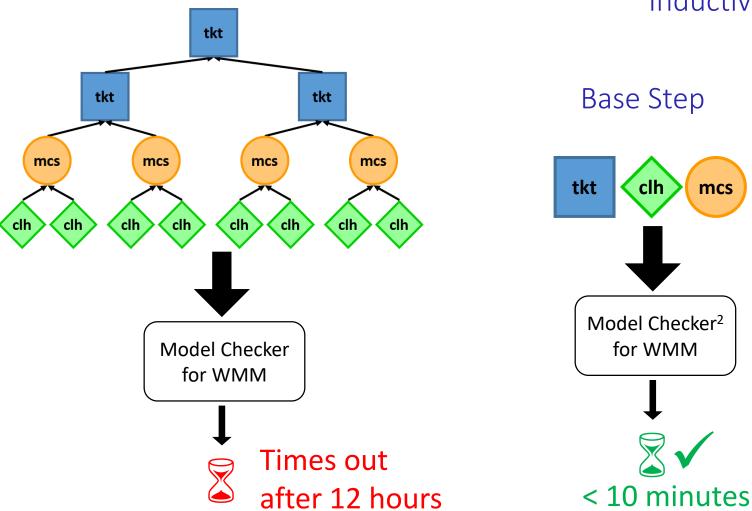
mcs

clh

for WMM

Inductive Step

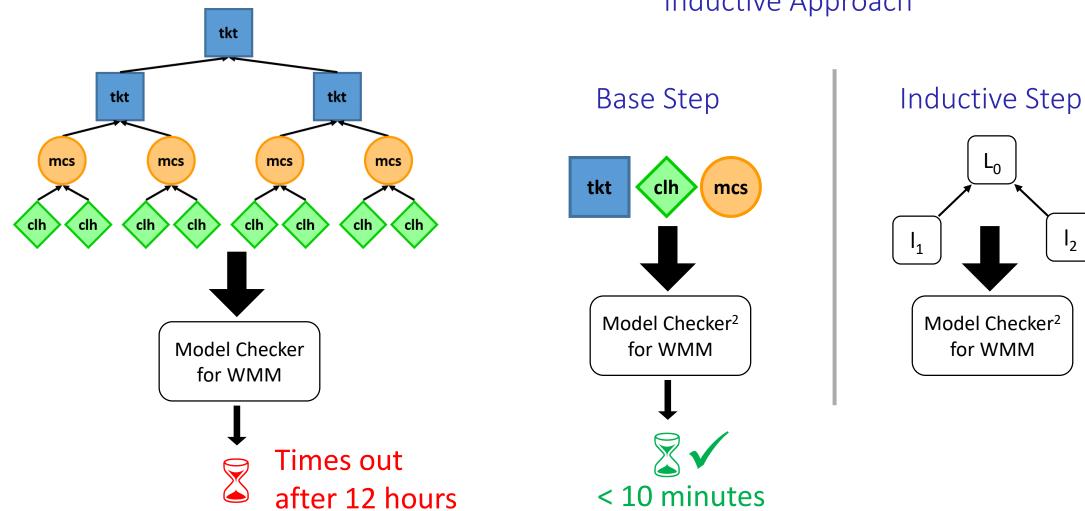
2_{Oberhauser et al.}, VSync: push-button verification and optimization for synchronization primitives on weak memory models, ASPLOS'2021



Inductive Approach

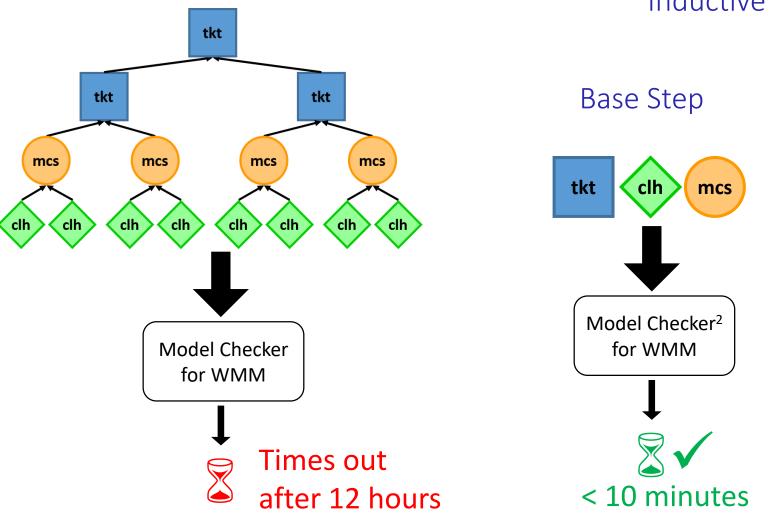
Inductive Step

2_{Oberhauser} et al., VSync: push-button verification and optimization for synchronization primitives on weak memory models, ASPLOS'2021

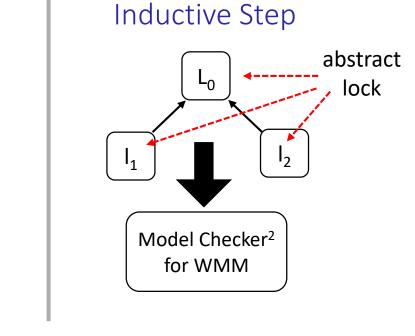


Inductive Approach

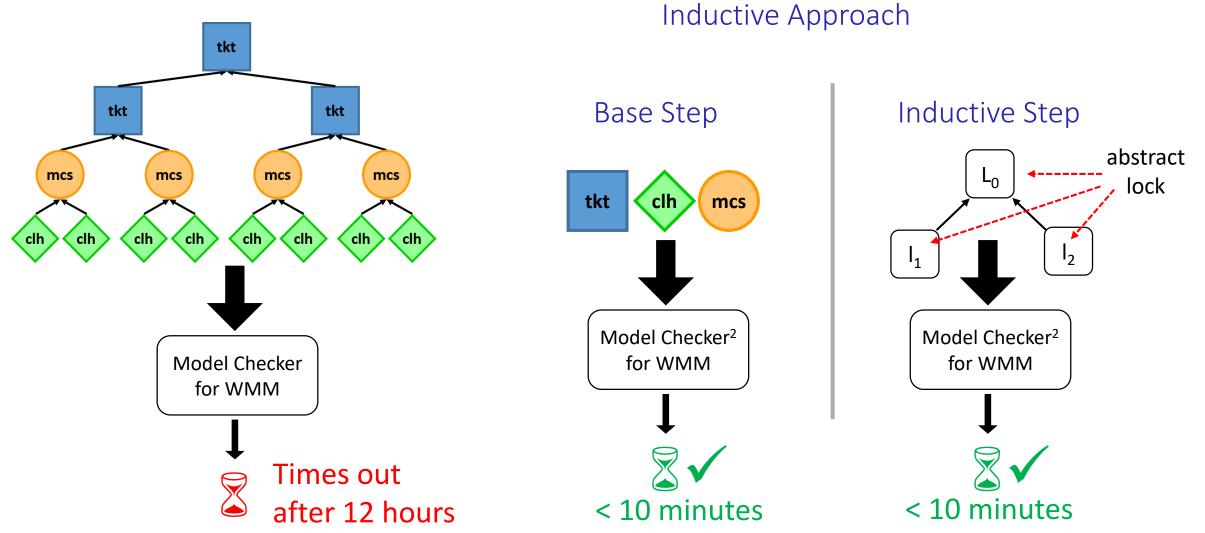
2_{Oberhauser} et al., VSync: push-button verification and optimization for synchronization primitives on weak memory models, ASPLOS'2021



Inductive Approach



2_{Oberhauser} et al., VSync: push-button verification and optimization for synchronization primitives on weak memory models, ASPLOS'2021



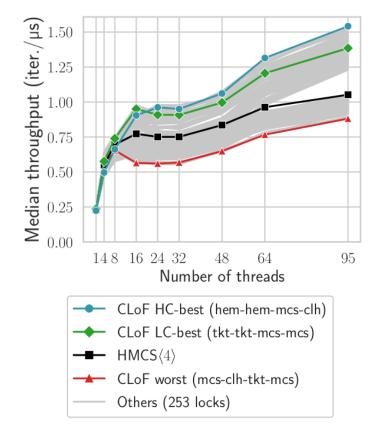
2_{Oberhauser et al.}, VSync: push-button verification and optimization for synchronization primitives on weak memory models, ASPLOS'2021



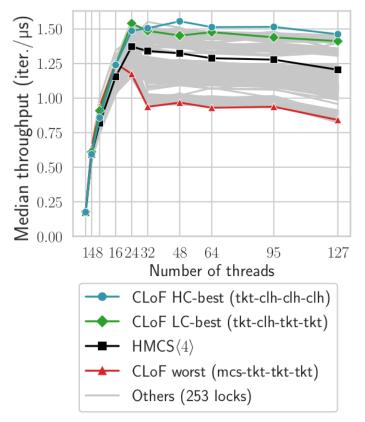
- How to figure out the hierarchy we need to use?
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- Run all lock combinations composed by the CLoF lock generator
- For B = 4 locks and L = 4 levels, we have $B^{L} = 4^{4} = 256$ combinations
 - Up to 1 hour in a platform with 128 cores

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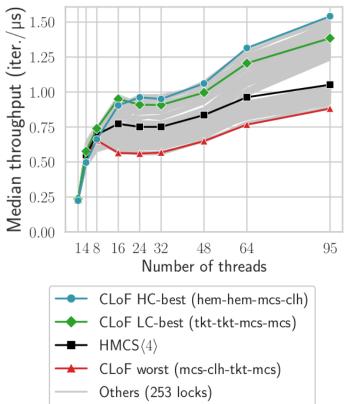


x86 server – levelDB readrandom benchmark

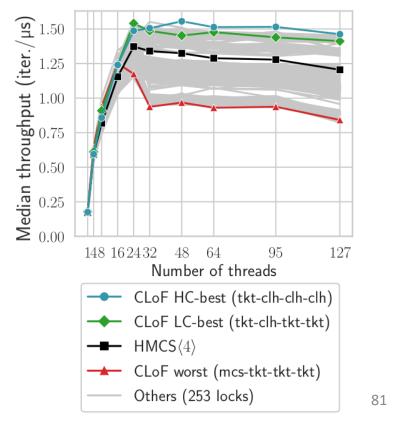


- Run all lock combinations composed by the CLoF lock generator ٠
- For B = 4 locks and L = 4 levels, we have $B^{L} = 4^{4} = 256$ combinations ٠
 - Up to 1 hour in a platform with 128 cores ٠

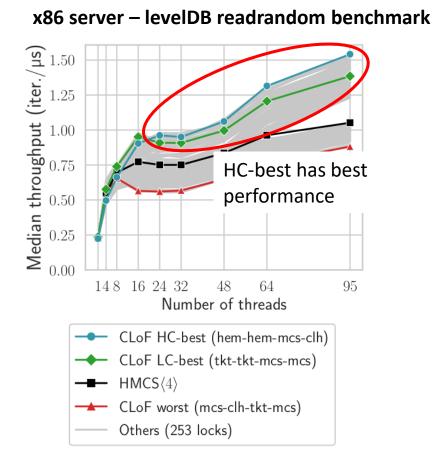
x86 server – levelDB readrandom benchmark



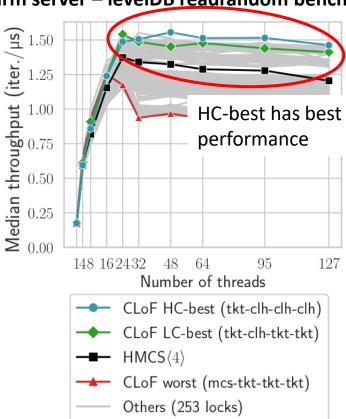
No combination is better for all contention levels



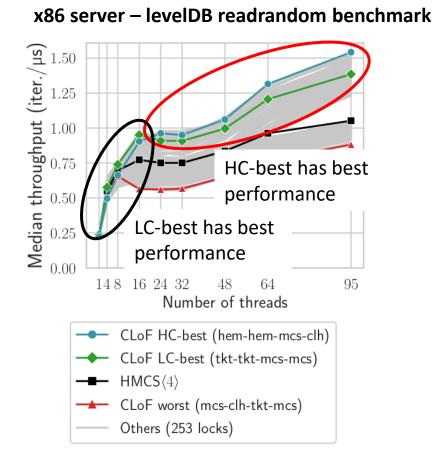
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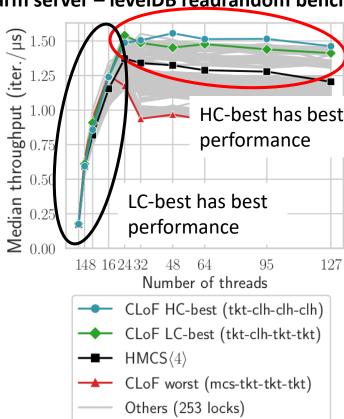
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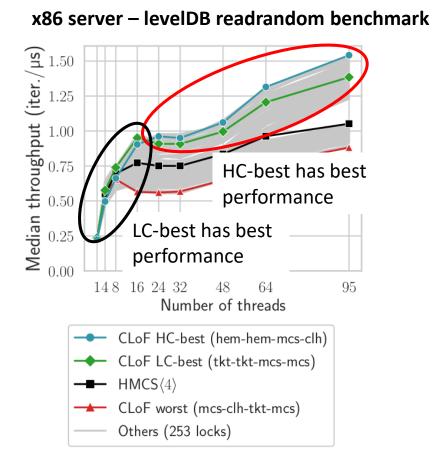
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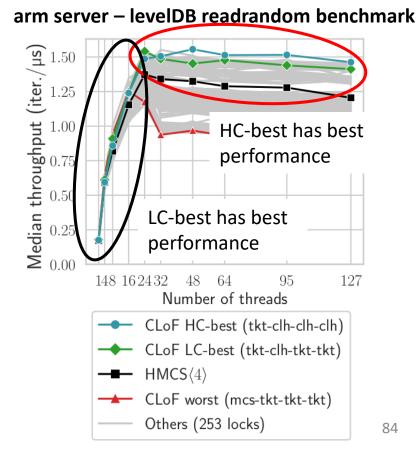


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- For B = 4 locks and L = 4 levels, we have $B^{L} = 4^{4} = 256$ combinations
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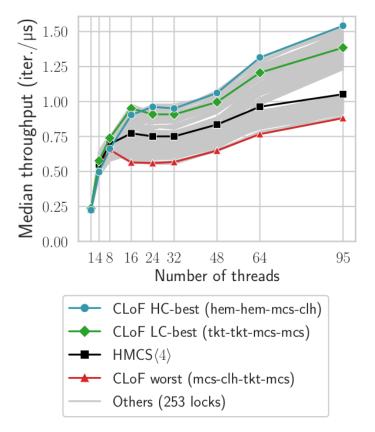


No combination is better for all contention levels

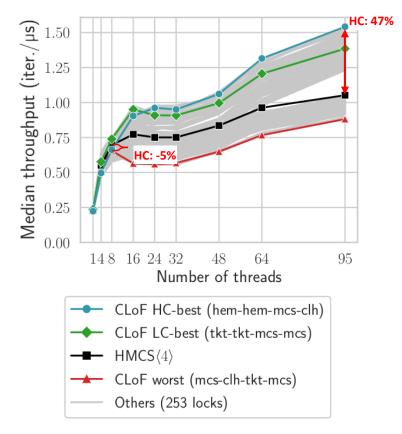
Which one should be chosen?



- CLoF stablishes 2 selection policies for the best lock:
 - HC-best prioritizes performance at high contention
 - LC-best prioritizes performance at low contention

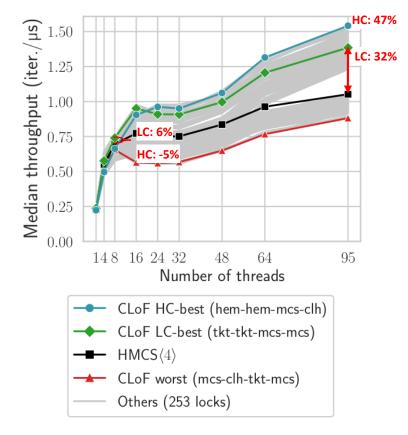


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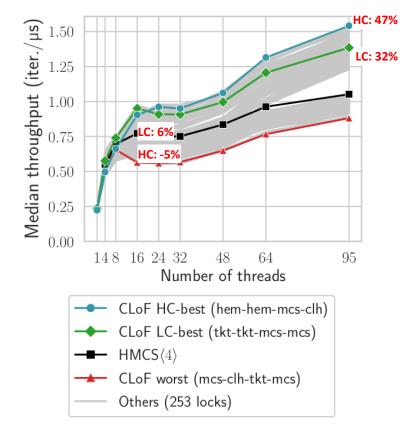


- CLoF stablishes 2 selection policies for the best lock:
 - HC-best prioritizes performance at high contention
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User can tune which selection policy is desired

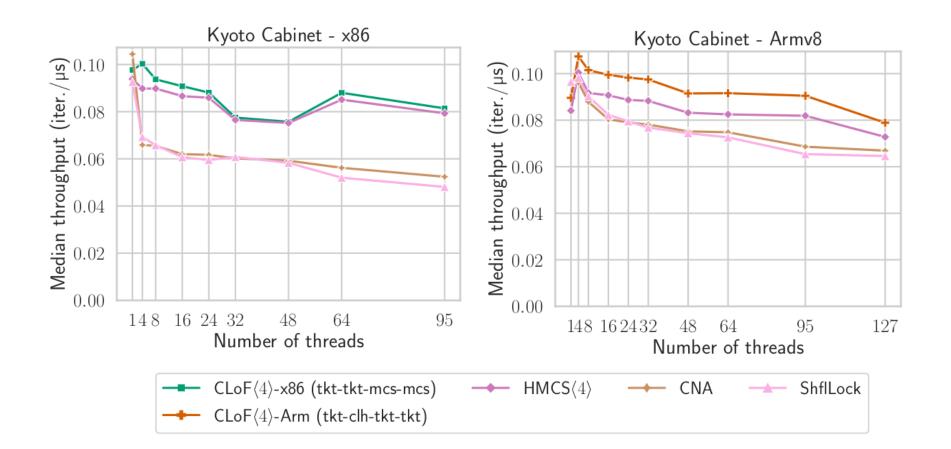
• Without the need to re-run the benchmark





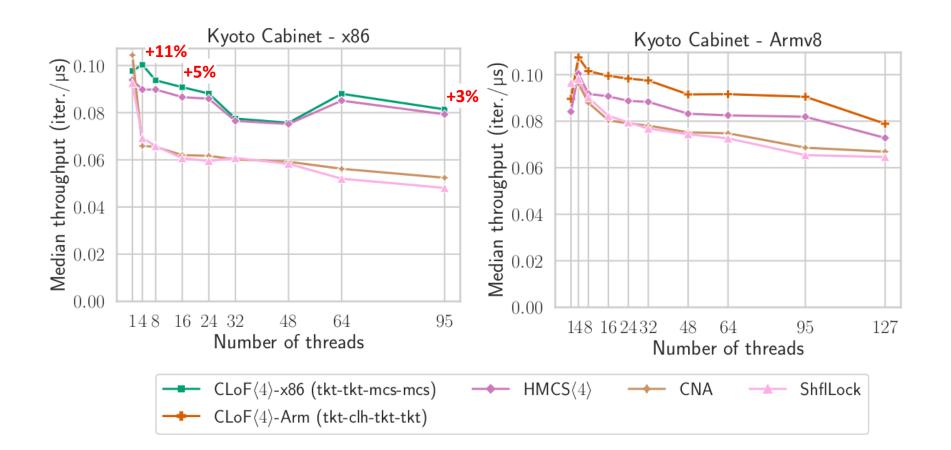
Evaluation

- Another benchmark, called Kyoto Cabinet, is used to cross-validate results
 - Display LC-best



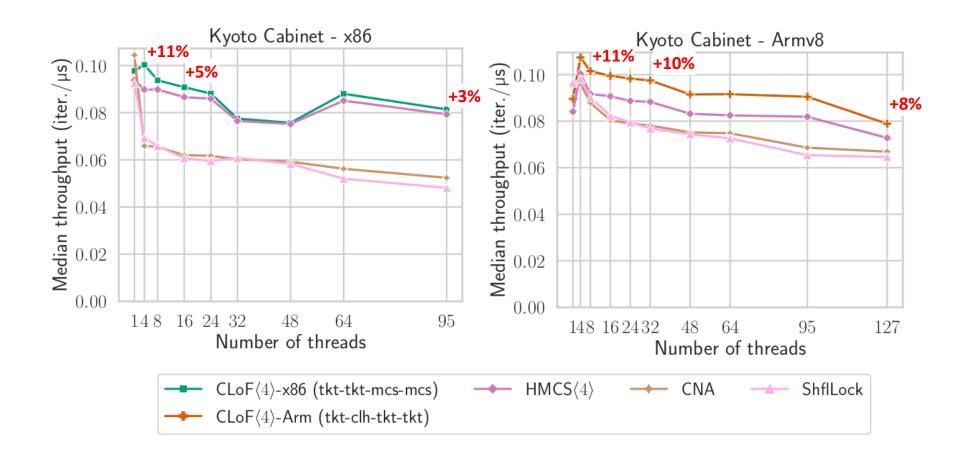
Evaluation

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Evaluation

- Another benchmark, called Kyoto Cabinet, is used to cross-validate results
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Conclusion and Future Work

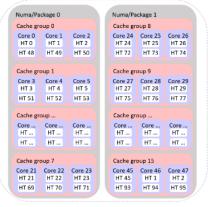
- CLoF locks
 - fully leverage deep hierarchy
 - are level heterogeneity
 - can be optimized for target platform
 - are correct-by-construction on Weak Memory Models
- Don't miss the details!
 - platform-specific optimizations
 - analysis of lock combinations
 - ...
- Future work
 - CLoF in the Linux kernel
 - big.LITTLE platforms

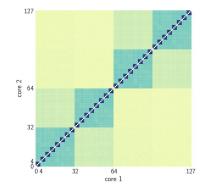
Thanks!

Tuning Point: Choosing the Hierarchy Levels

- Not all levels will always be used
 - Application can disable hyperthreads x86 server

٠	Some levels may	have small improveme	ent – package leve	on Kunpeng 920





Tuning Point: Choosing the Hierarchy Levels

- Not all levels will always be used
 - Application can disable hyperthreads x86 server

•	Some levels may	have small improvement	– package level	on Kunpeng 920
				1 0

- User can tune levels that are wanted
 - Include/Remove levels found at discovery

							· · · · · · · · · · · · · · · · · · ·	
1	Numa/Package 0		Numa/Package 1					
	Cache group 0				Cache group 8			
	Core 0 HT 0	Core 1 HT 1	Core 2 HT 2		Core 24 HT 24	Core 25 HT 25	Core 26 HT 26	
	HT 48	HT 49	HT 50		HT 72	HT 73	HT 74	
	Cache group 1				Cache group 9			
	Core 3 HT 3	Core 4 HT 4	Core 5 HT 5		Core 27 HT 27	Core 28 HT 28	Core 29 HT 29	
	HT 51	HT 52	HT 53		HT 75	HT 76	HT 77	
	Casha as				Casha an			
	Cache gr	· · · · ·			Cache group			
	Core HT	Core HT	Core HT		Core HT	Core HT	Core HT	
	HT	HT	HT		HT	HT	HT	
	Cache group 7				Cache gr	oup 15		
	Core 21 HT 21	Core 22 HT 22	Core 23 HT 23		Core 45 HT 45	Core 46 HT 1	Core 47 HT 2	
	HT 69	HT 70	HT 71		HT 93	HT 94	HT 95	

