

# Challenges Implementing Software-Defined Virtual Memory

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Virtual memory management hardware, and especially a MMU's translation lookaside buffer (TLB), contribute up to 15-20% to the energy consumption of a modern CPU. The major contributors to this energy consumption are the comparators required to realize the TLB's content-addressable memory and the hardware page table walks to handle a TLB miss.

While numerous ideas have been proposed to increase the energy efficiency of virtual memory subsystems, these commonly require hardware modifications not present in off-the-shelf CPUs. On the other hand, emulation and virtualization solutions already support some sort of software-implemented MMU implementation, which often already is optimized for performance.

In this talk, we discuss the possibility of implementing virtual memory management for regular user mode processes purely in software, i.e. without the involvement of memory translation hardware. In order to achieve this, we propose to use a same-ISA just-in-time (JIT) binary translation system for user mode processes which validates and rewrites code and data addresses generated by a program into physical memory addresses during translation.

There are significant challenges for an efficient implementation of this software-based approach. In addition to achieving the primary objective of energy reduction, other challenges to solve involve the latencies when looking up page table entries and the execution time overhead involved in checking the validity of an address - but also the security of a JIT approach needs to be considered. The talk will discuss these challenges and some solution approaches.