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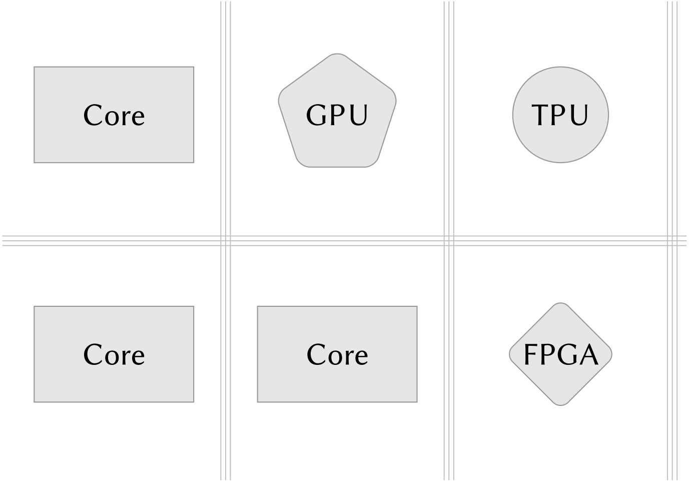
Efficient and Scalable Core Multiplexing with M^{3}v

Nils Asmussen, Sebastian Haas, Carsten Weinhold, Till Miemietz, Michael Roitzsch

Fachgruppentreffen, Erlangen, 19.09.2022

M3 System Architecture [1]



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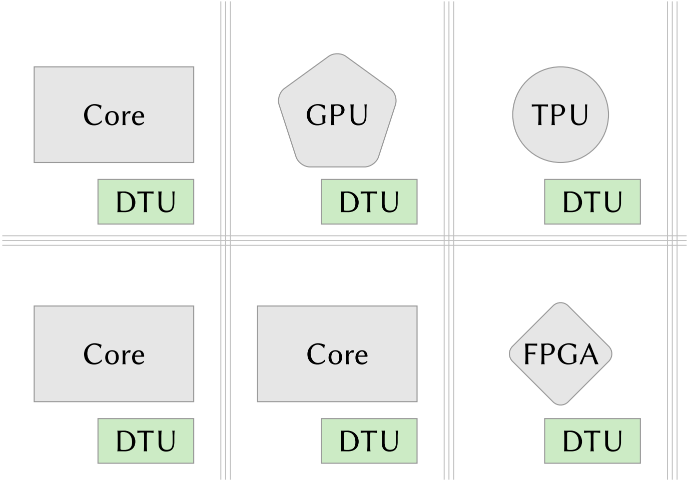

Key ideas:

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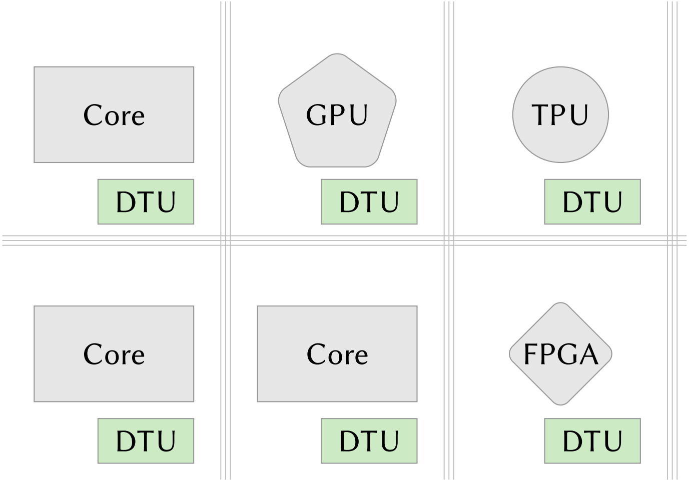

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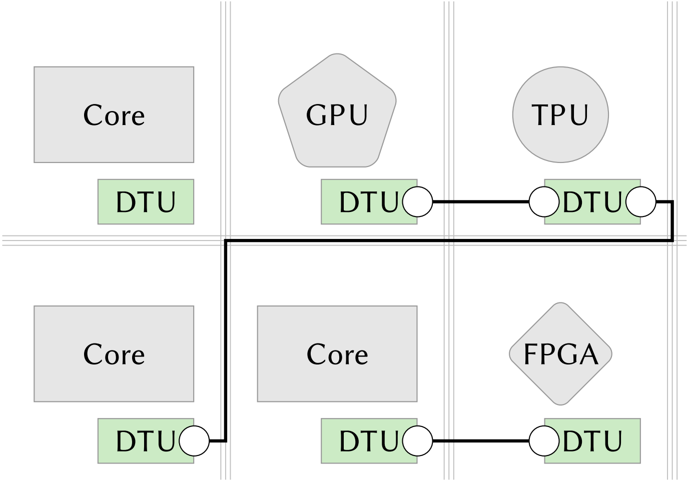

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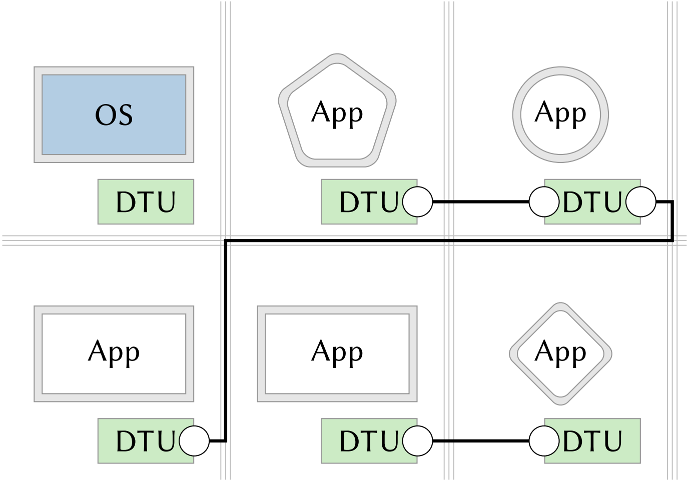

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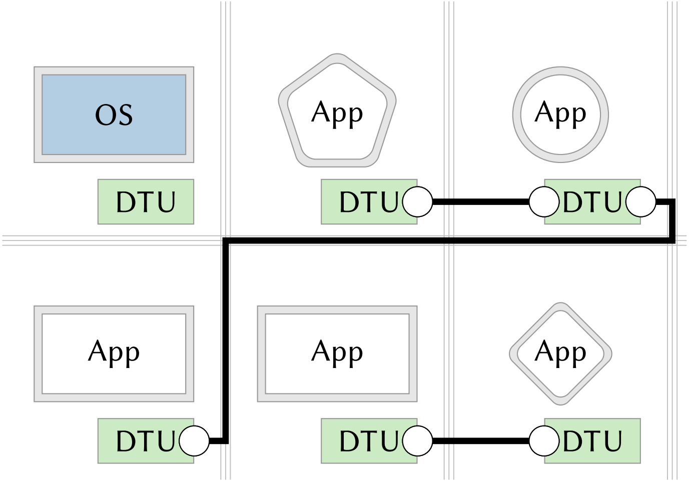

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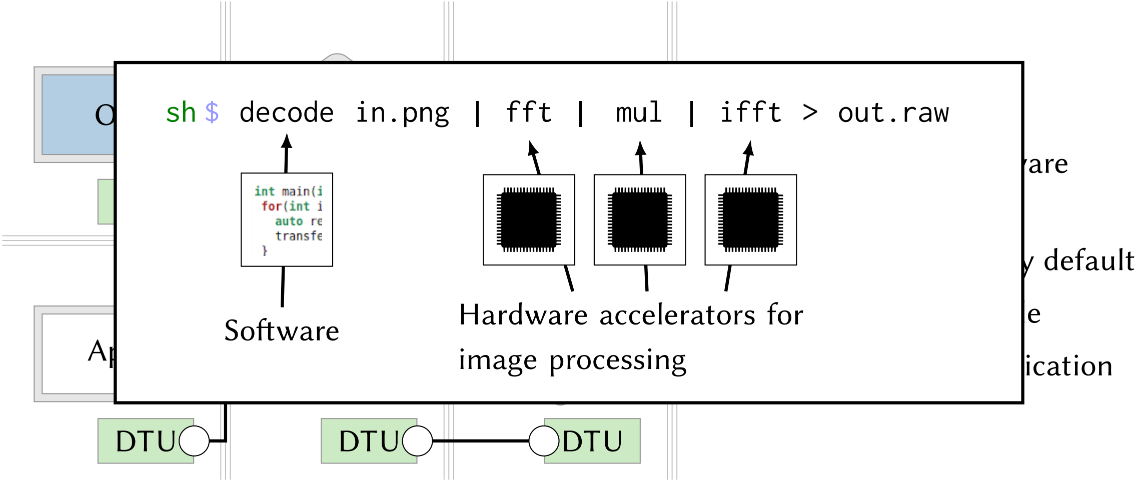

```
sh $ decode in.png | fft | mul | ifft > out.raw
```

```
int main(i
 for(int i
   auto re
   transfe
 }
```

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Comparison of Core Multiplexing Approaches

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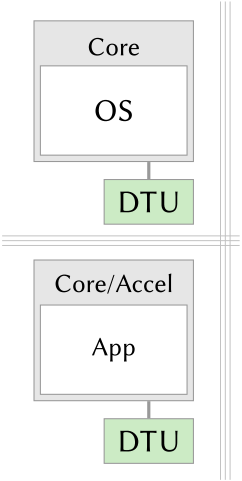

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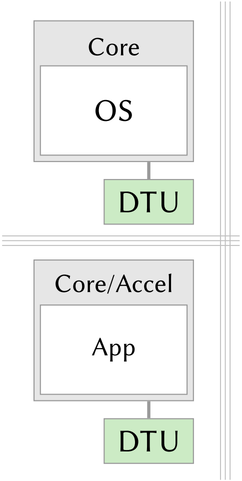
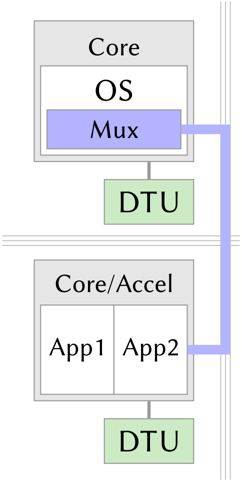


M^{3}x (ATC’19)



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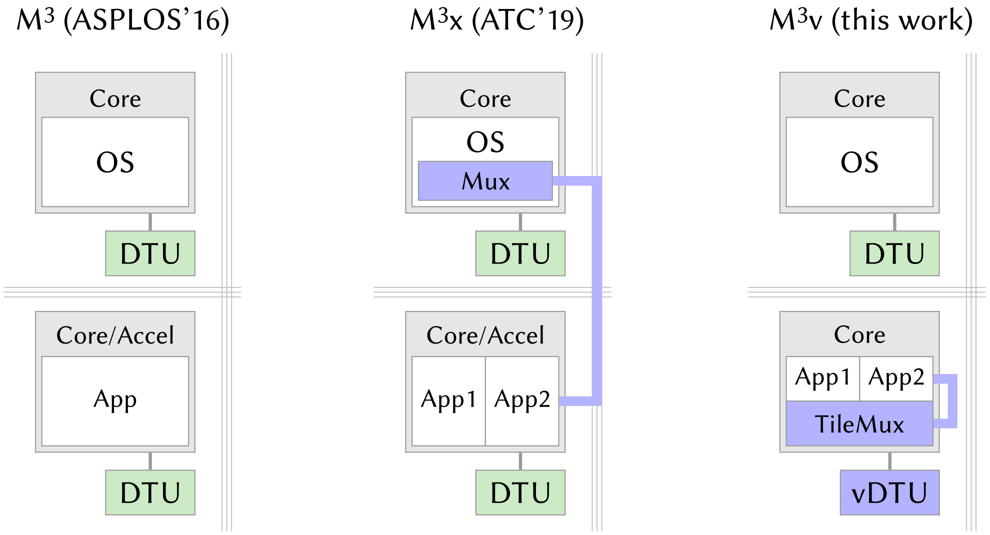
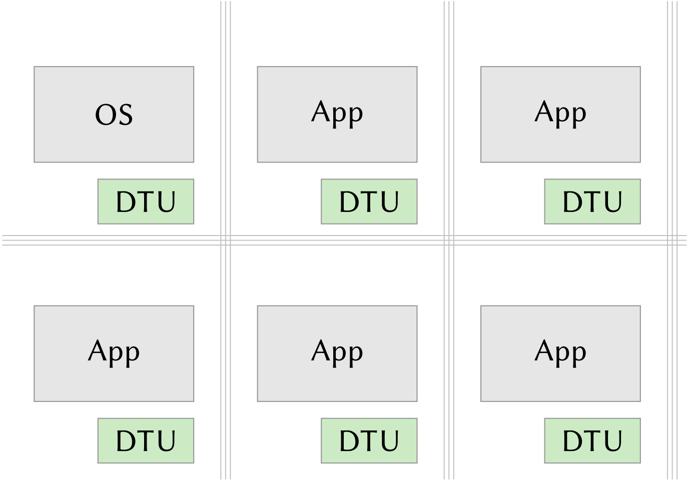


Core Multiplexing vs Fast-Path Communication



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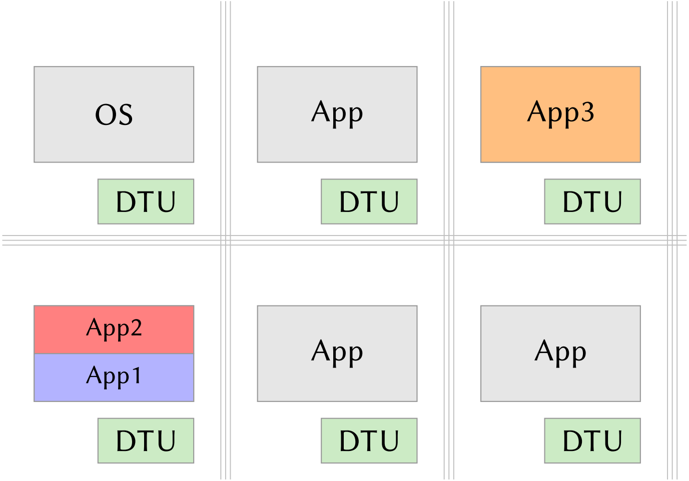

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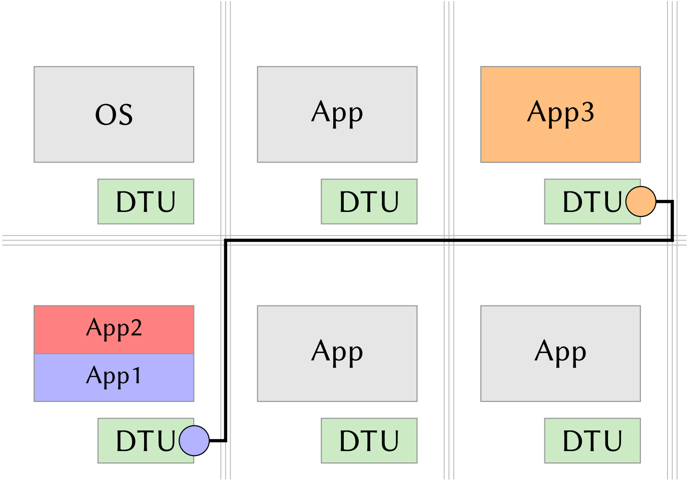

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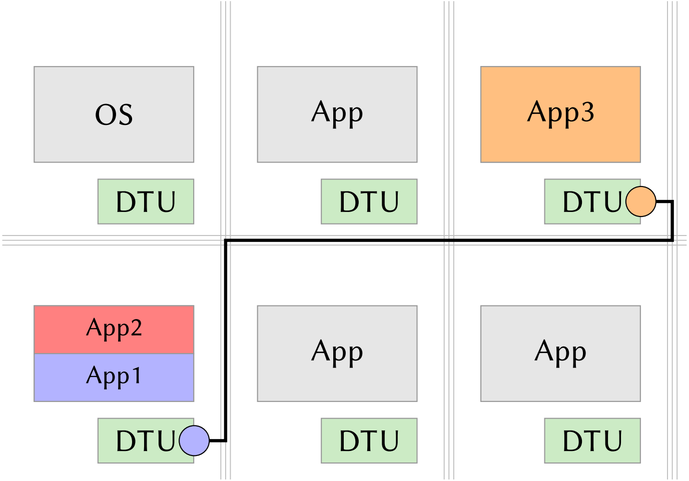

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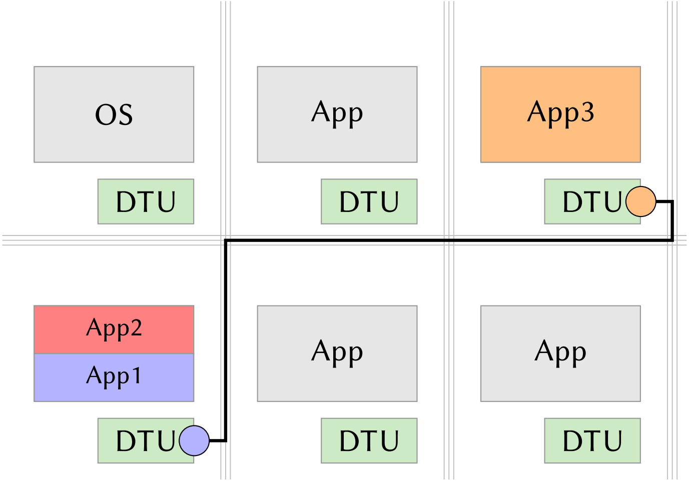

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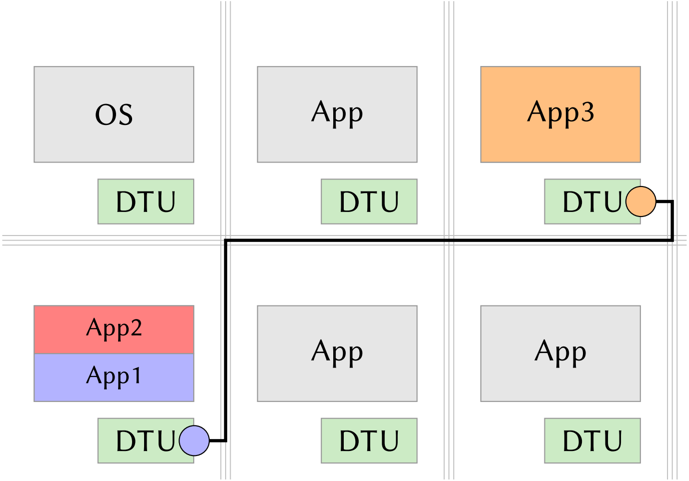

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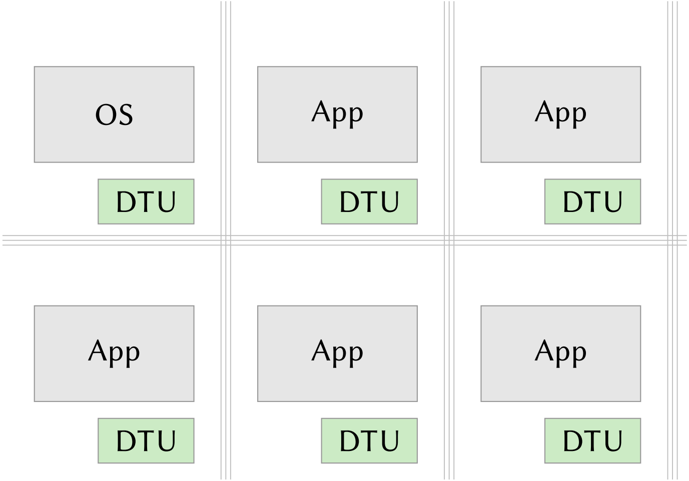
- Multiplexing conflicts with fast-path communication

Strong Isolation between Tiles



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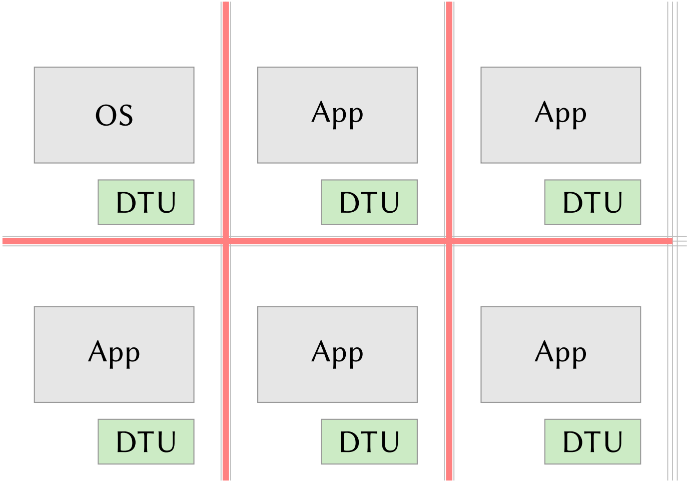

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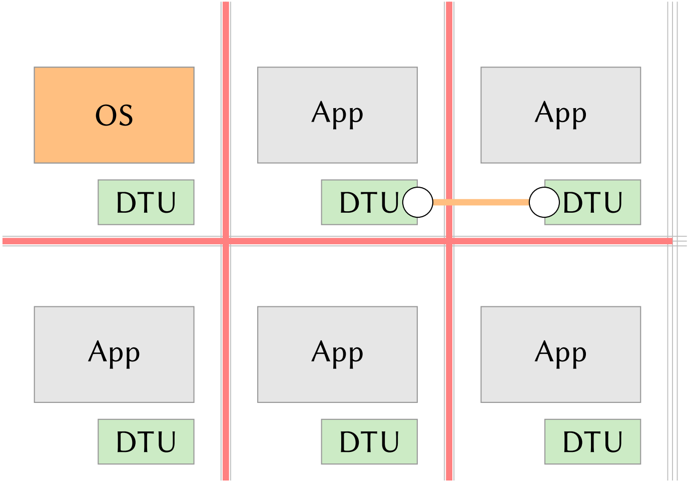

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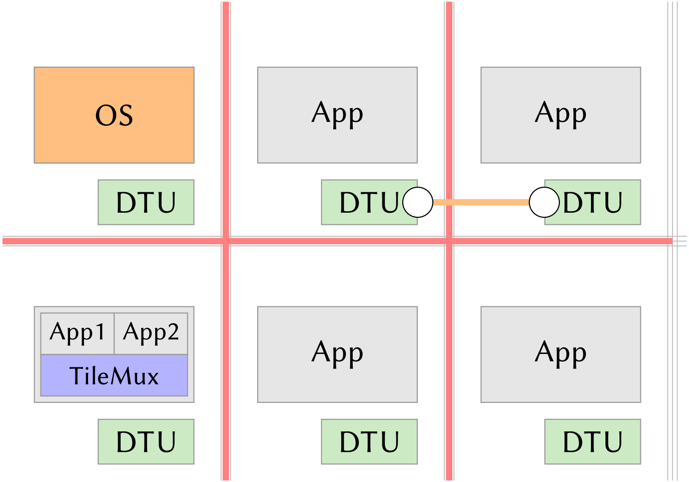

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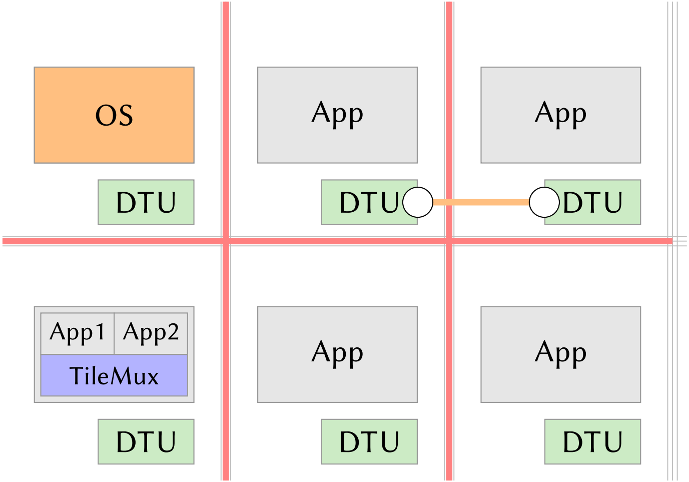

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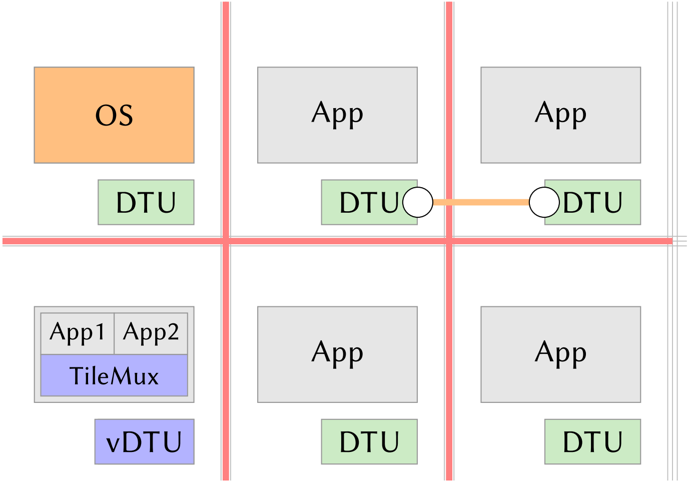

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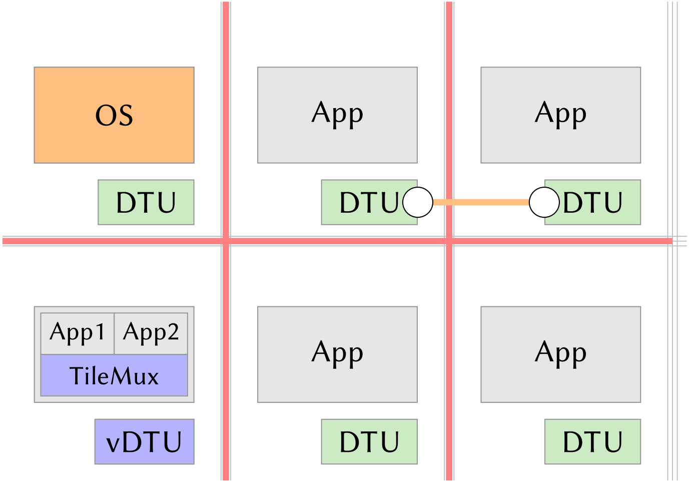

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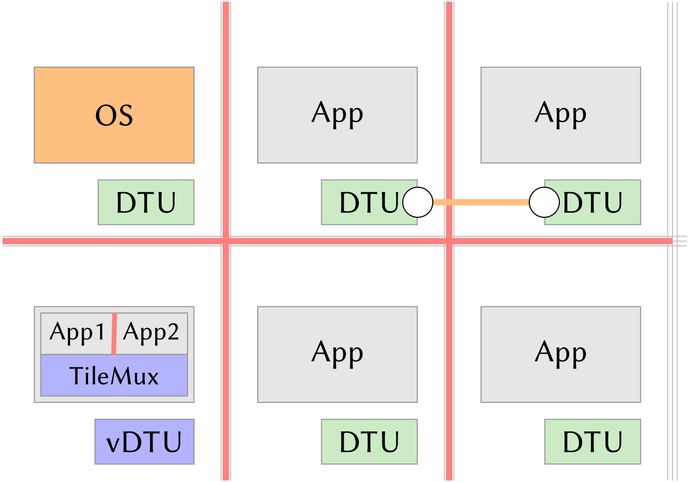

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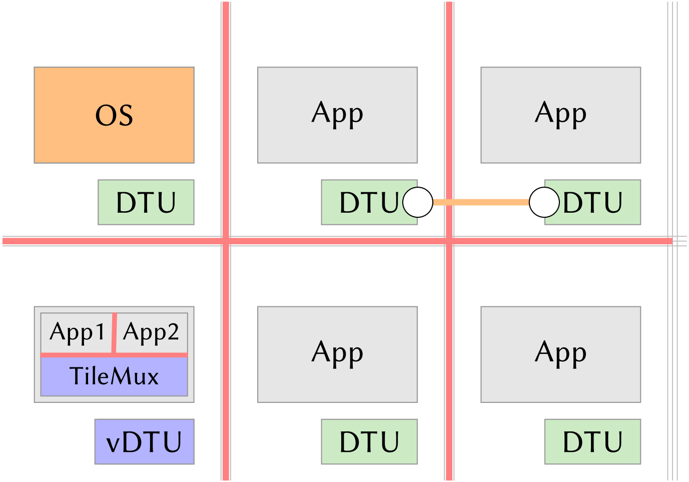

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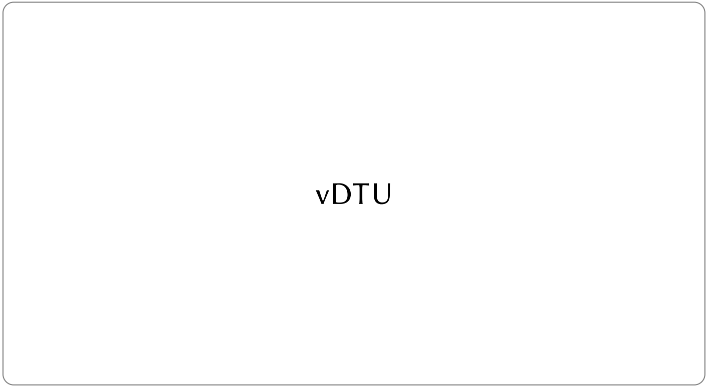
- M3v trades some more isolation for better efficiency

Virtualization of the DTU



vDTU

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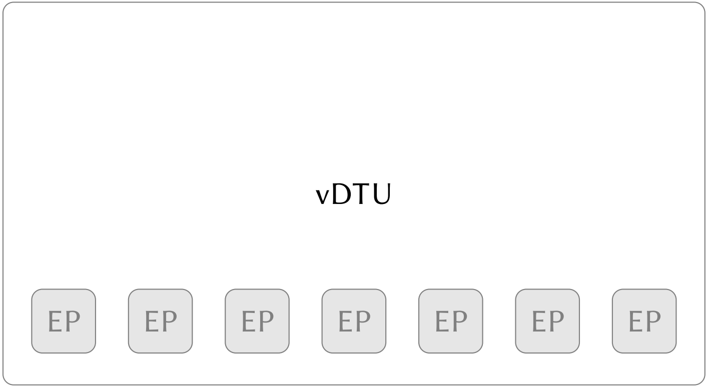

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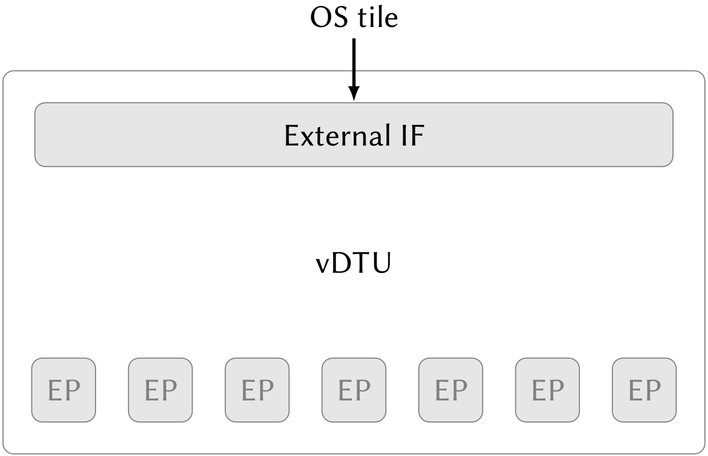

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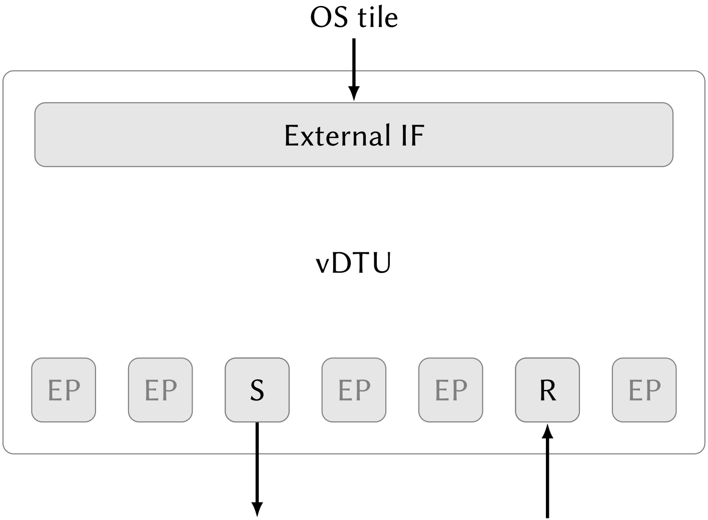

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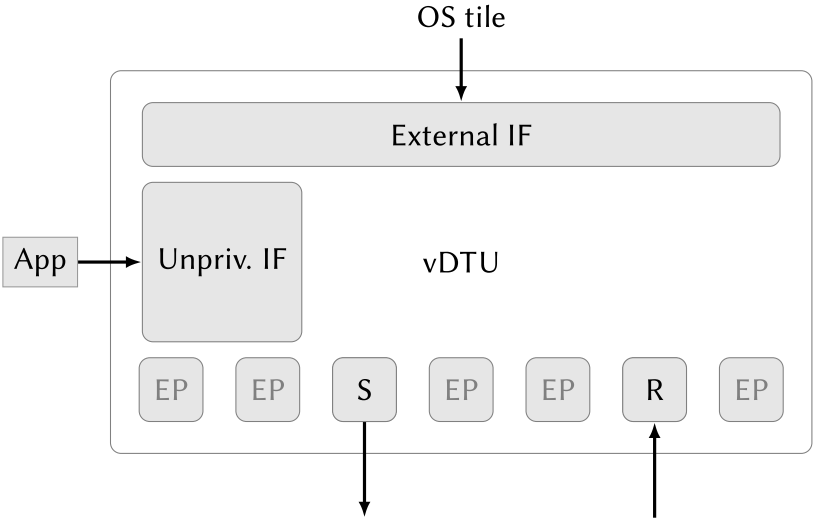

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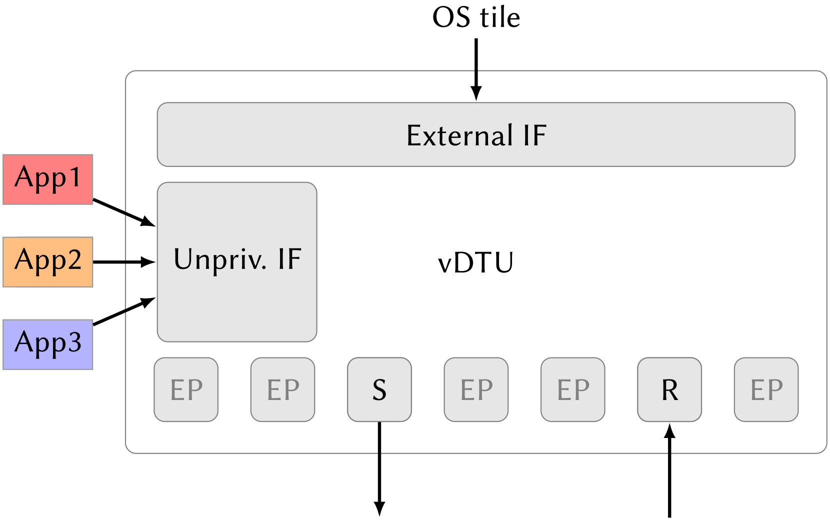

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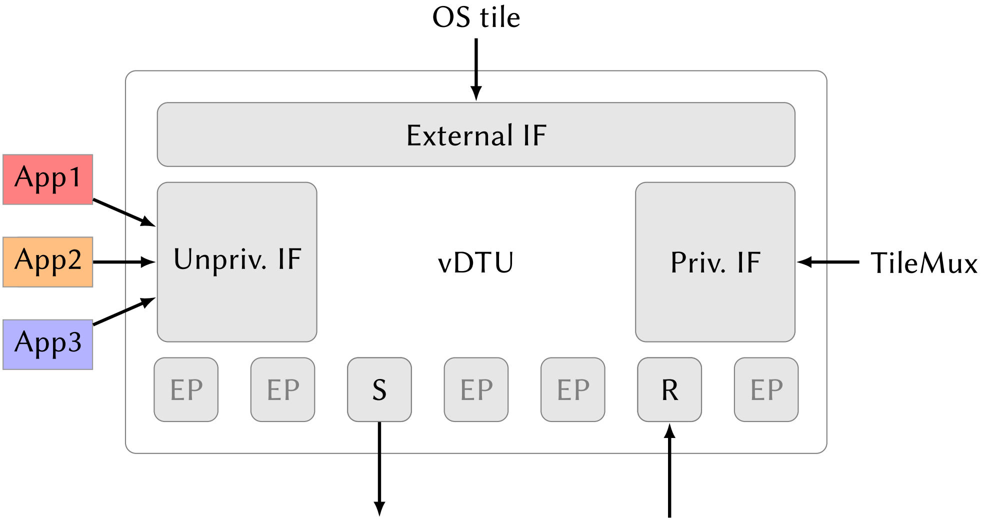

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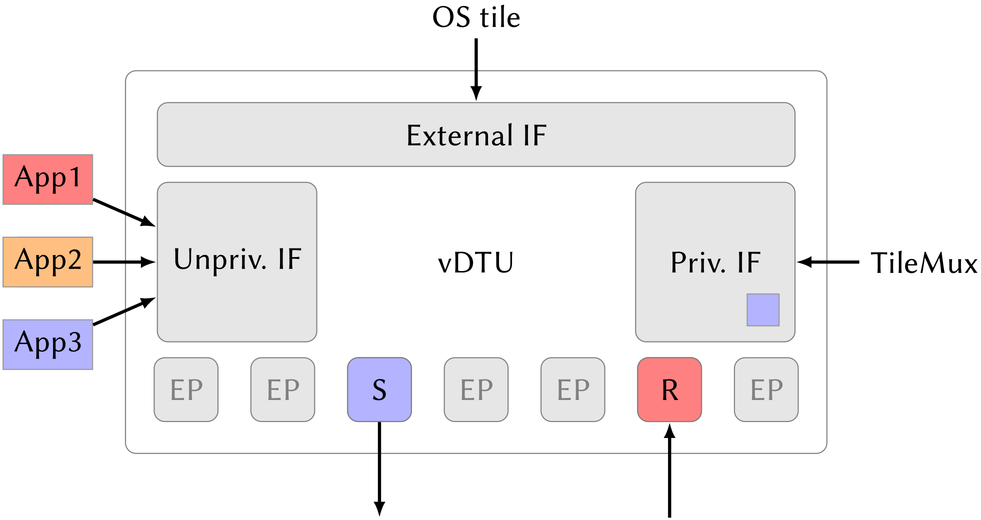

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- TileMux marks the receiver as ready
- Best case: neither the OS tile nor TileMux is involved in the communication

Performance/Scalability Comparison with M^3x

- Setup: gem5 simulator, 3 GHz out-of-order x86-64 cores
- Every tile runs: SQLite/find benchmark and in-memory filesystem

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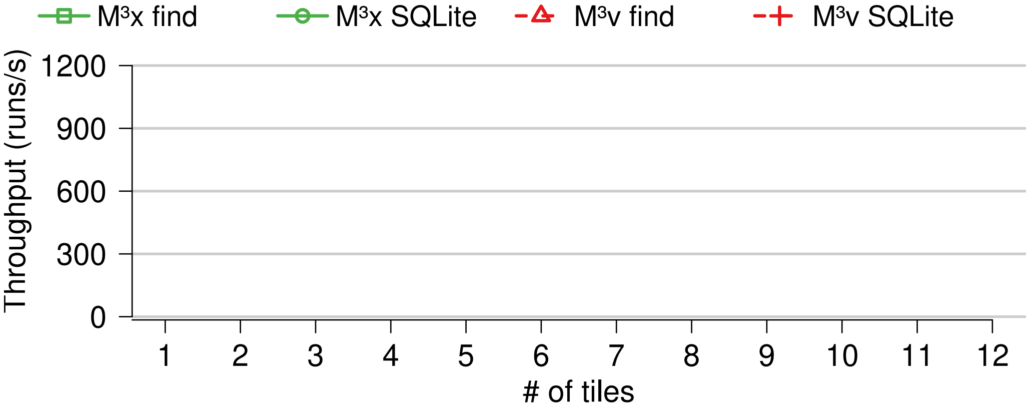

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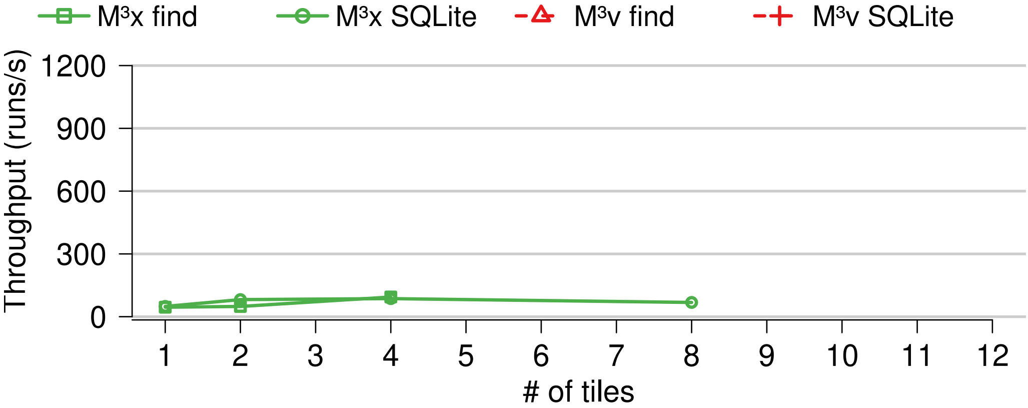

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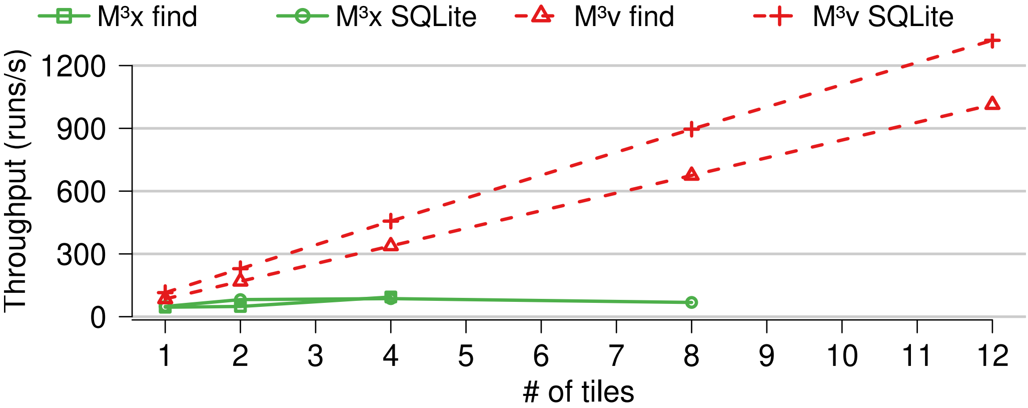

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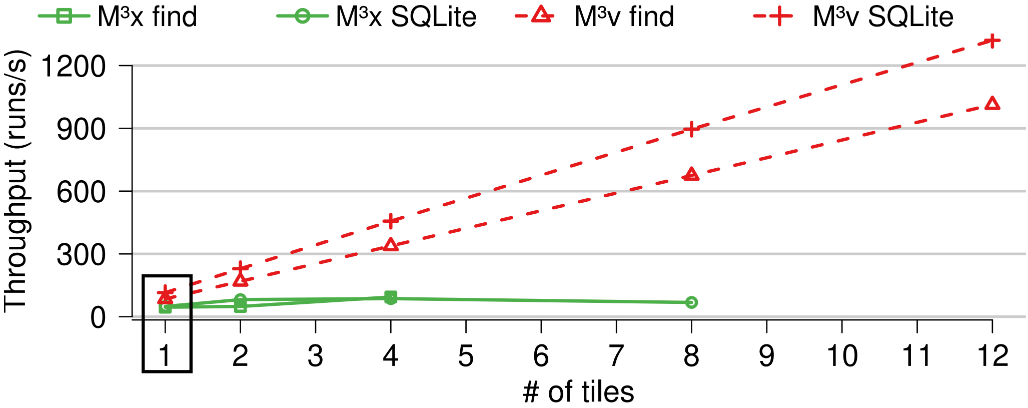

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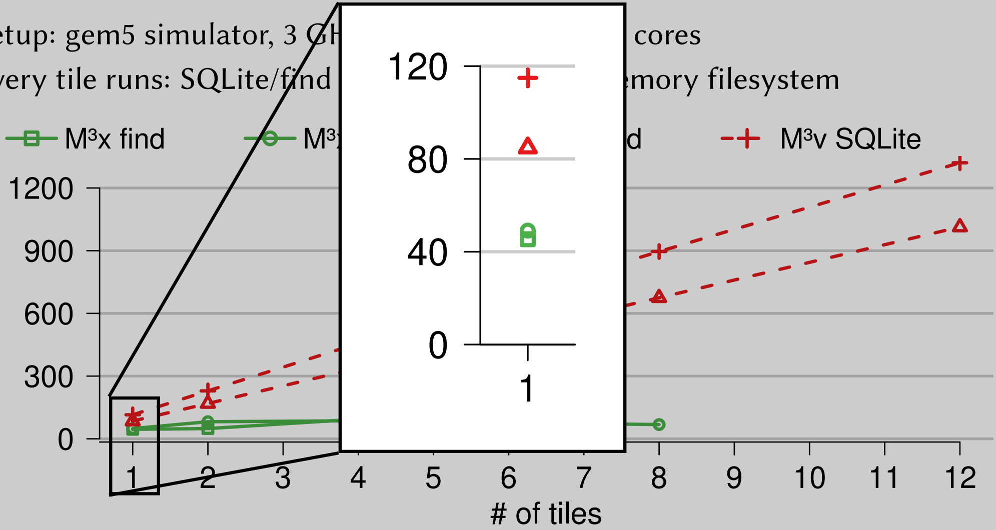

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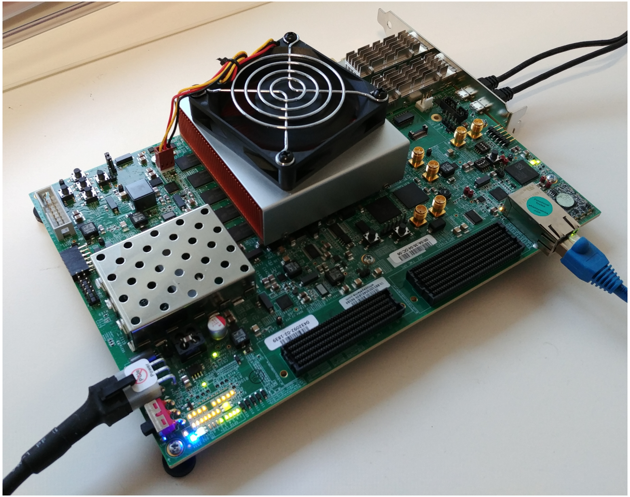

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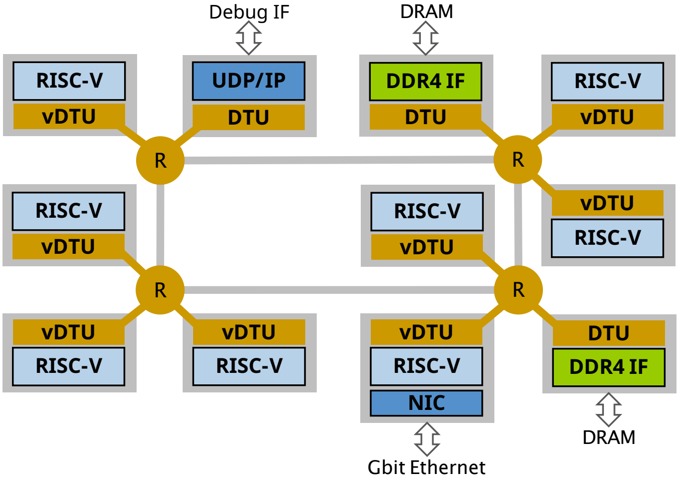

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- RISC-V: in-order Rocket or out-of-order BOOM
- Rocket at 100 MHz, BOOM at 80 MHz
- 2x16 kB L1, 512 kB L2
- vDTU contains 128 EPs

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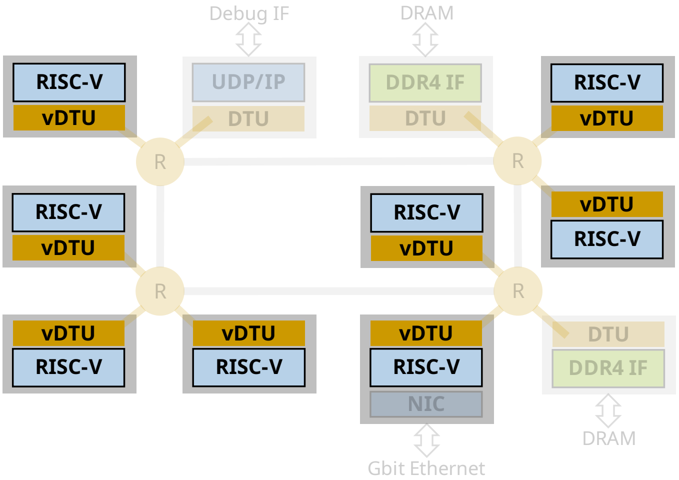

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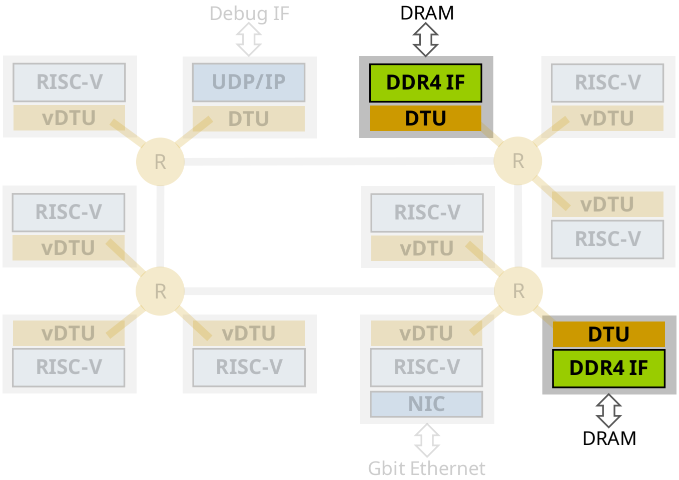

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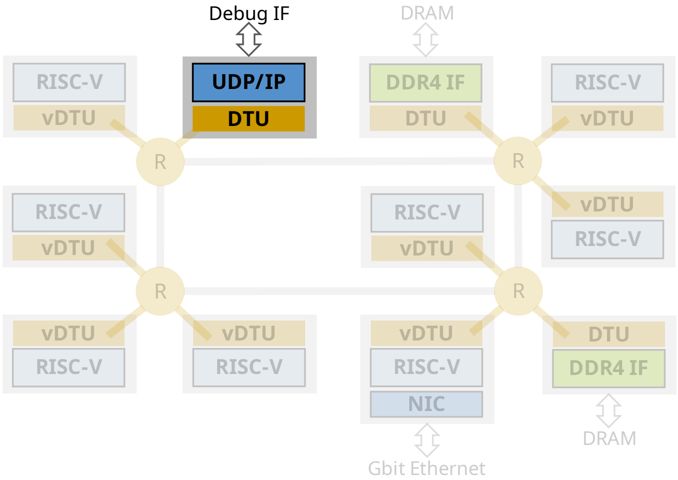

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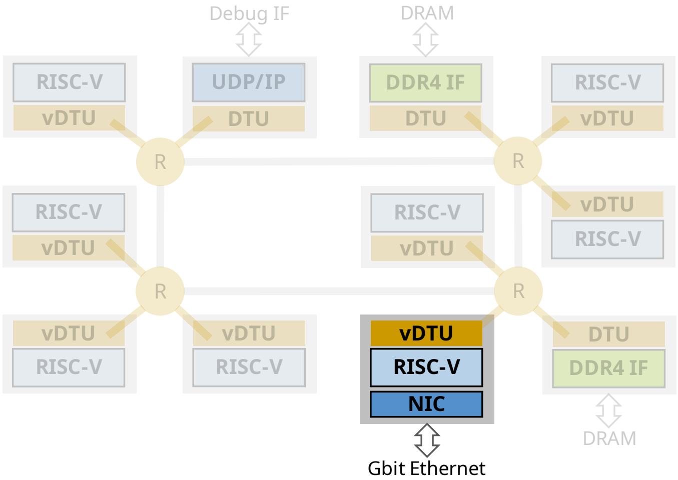

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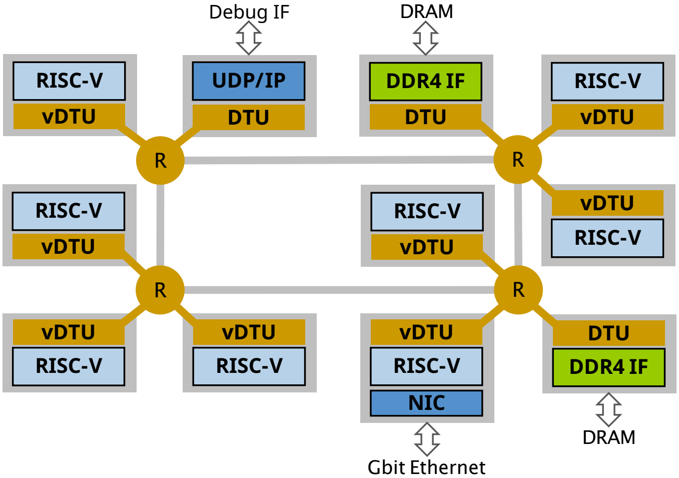

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vDTU Size and Complexity

	LUTs [k]	**FFs [k]**	**BRAMs**
BOOM	143.8	71.8	159
Rocket	46.6	22.0	152
NoC router	3.4	2.2	0
vDTU	15.2	5.8	0.5
Control Unit	10.3	3.3	0.5
NoC CTRL	3.2	1.5	0
CMD CTRL	7.1	2.8	0.5
Unpriv. IF	6.2	2.5	0.5
Priv. IF	0.9	0.3	0
Register file	2.0	1.0	0
Memory mapper + PMP	0.6	0.2	0
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BOOM	143.8	71.8	159
Rocket	46.6	22.0	152
NoC router	3.4	2.2	0
vDTU	15.2	5.8	0.5
Control Unit	10.3	3.3	0.5
NoC CTRL	3.2	1.5	0
CMD CTRL	7.1	2.8	0.5
Unpriv. IF	6.2	2.5	0.5
Priv. IF	0.9	0.3	0
Register file	2.0	1.0	0
Memory mapper + PMP	0.6	0.2	0
I/O FIFOs	2.3	0.3	0

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Performance Comparison with Linux

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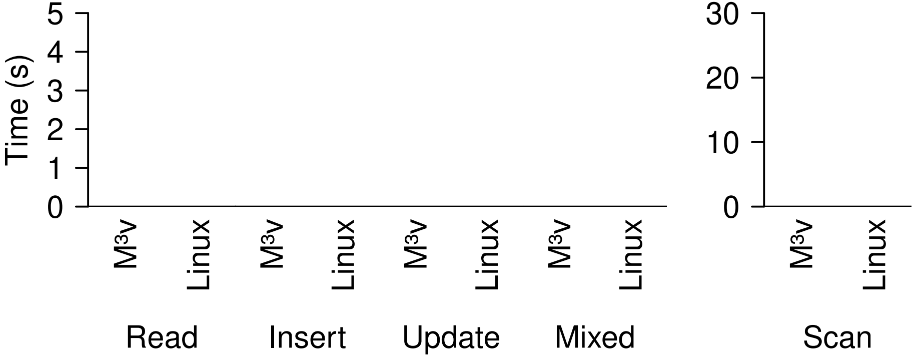

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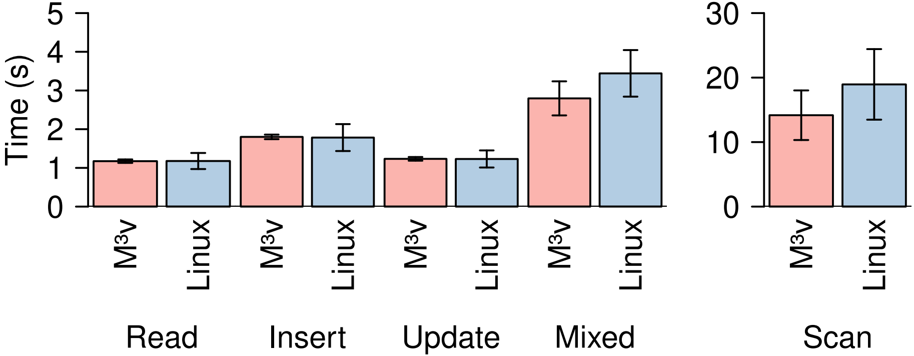
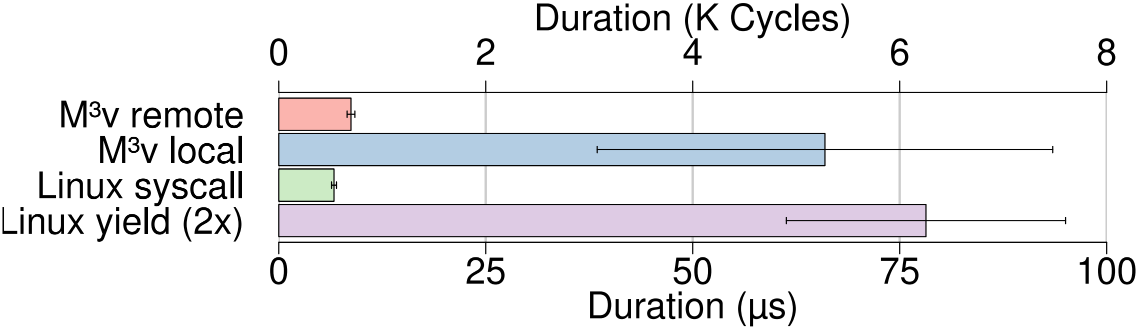


Conclusion

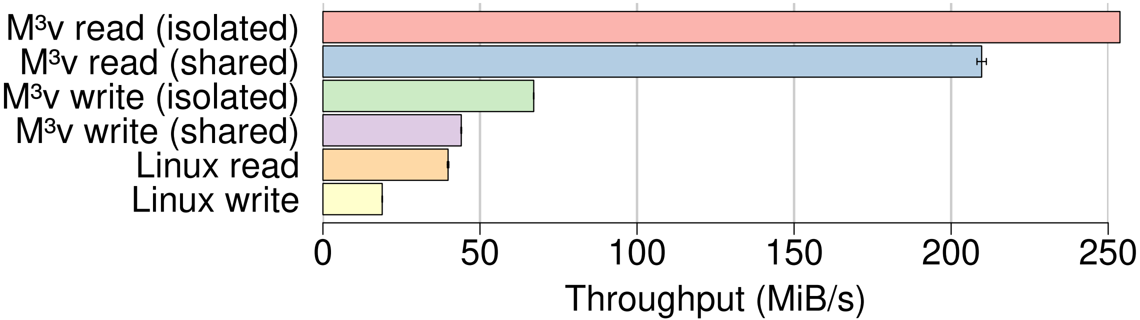
- M^3 explores a new system architecture with a new per-tile hardware component
- M^{3}v shows how general-purpose cores can be multiplexed efficiently
- Hardware implementation demonstrates modest additional hardware costs
- Competitive performance to Linux with context-switch-heavy workloads
- The complete hardware/software stack is available as open source: `https://github.com/Barkhausen-Institut/M3`

Backup Slides

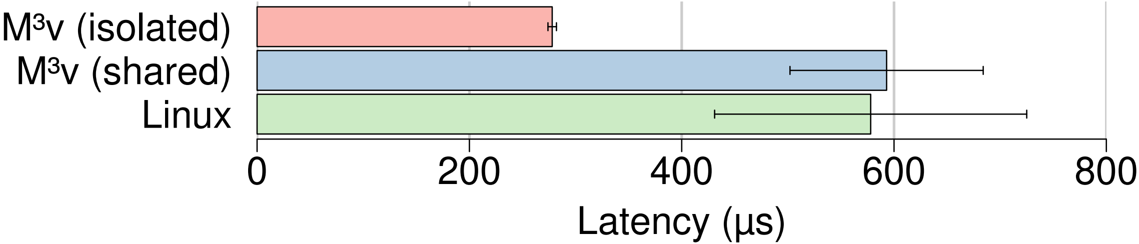
Microbenchmarks: IPC and Context Switches



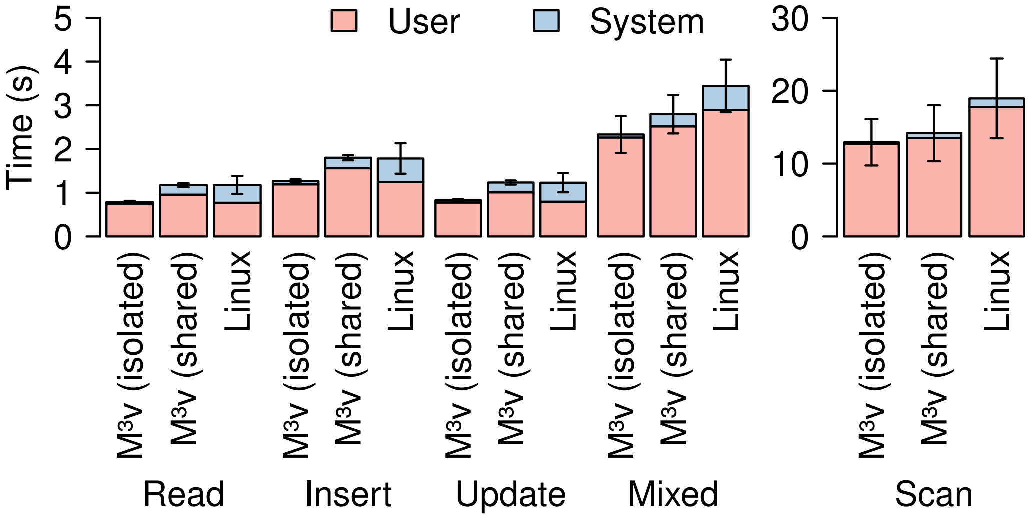
Microbenchmarks: File System



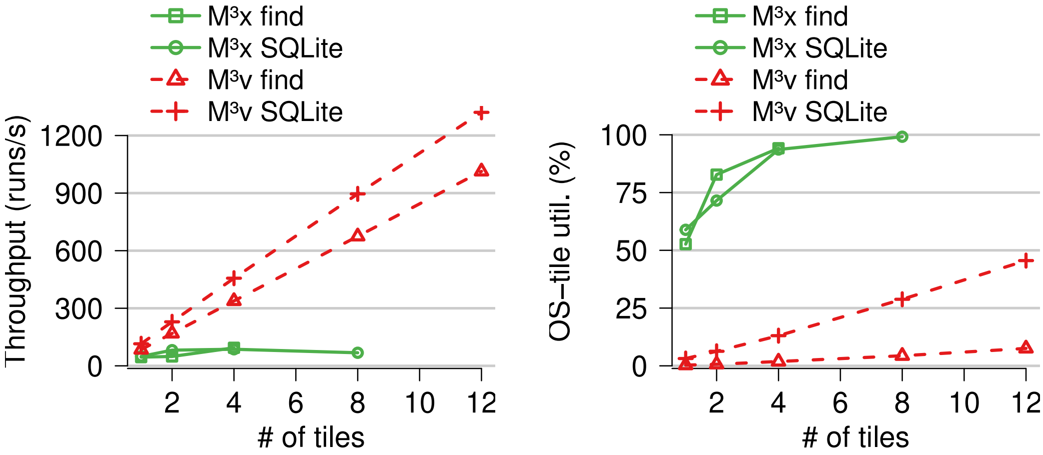
Microbenchmarks: Networking



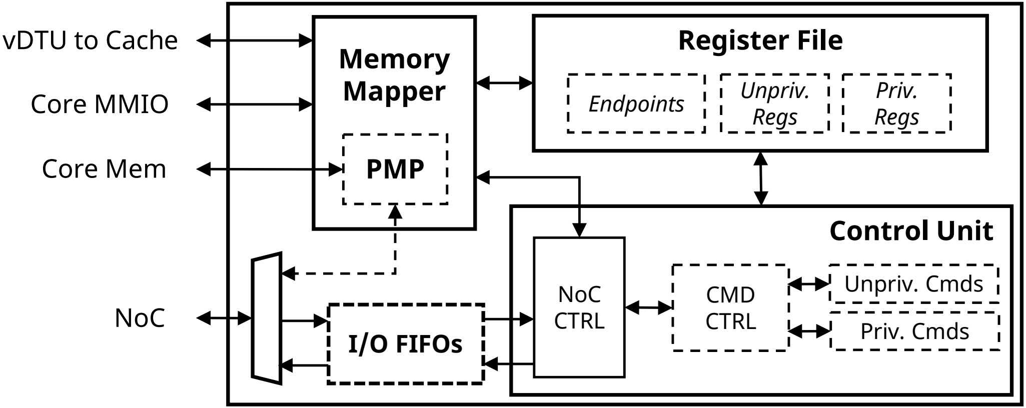
Macrobenchmarks: YCSB



Comparison with M³x: OS-tile utilization



Hardware Implementation


vDTU to Cache
Core MMIO
Core Mem
NoC
Memory Mapper
PMP
Register File
Endpoints
Unpriv. Regs
Priv. Regs
Control Unit
NoC CTRL
CMD CTRL
Unpriv. Cmds
Priv. Cmds
I/O FIFOs